Development of Monolithic SiGe and Packaged RF MEMS High-Linearity Five-bit High-Low Pass Phase Shifters for SOC X-band T/R Modules

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
in
Electrical and Computer Engineering

School of Electrical and Computer Engineering
Georgia Institute of Technology
August 2007

Development of Monolithic SiGe and Packaged RF MEMS High-Linearity Five-bit High-Low Pass Phase Shifters for SOC X-band T/R Modules

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For my parents...

ACKNOWLEDGEMENTS

This dissertation would not have been possible without the following people:

- My parents, Mark and Kathy Morton
- My family, and their unending support
- The Macallan family, for helping me recover from the long nights in the cleanroom
- Dr John Papapolymerou and Dr John Cressler for their advice and help with my research
- My fellow colleagues and friends at GEDC and the MiRC cleanroom
- The GEDC and MiRC cleanroom staff
- Kyle Bruner for helping with fabrication issues
- My sponsors: Georgia Electronic Design Center (GEDC), National Science Foundation (NSF), Georgia Tech Packaging Research Center (PRC), and the US Army and Missile Defense Agency.

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LIST OF SYMBOLS AND ABBREVIATIONS

$\sim$	approximately equal to
$>$	greater than
$<$	less than
$\mathring{A}$	angstrom = 10^{-10} meter
Au	gold
C	centigrade
CB-CPW	conductor backed coplanar waveguide
CPW	coplanar waveguide
CMOS	complementary-metal-oxide-semiconductor
CTE	coefficient of thermal expansion
Cr	chrome
Cu	copper
dB	decibel
dBm	decibels referenced to one milliwatt
dB	deep reactive ion etch
ϵ_r	dielectric constant
$\circ$	degrees
FET	field-effect transistor
fF	femto farads = 10^{-15} farads
f_o	center frequency or cut-off frequency or resonant frequency
ft	foot
GaAs	gallium-arsenide
GHz	gigahertz = 10^9 cycles per second
GPS	global positioning satellite
IL	insertion loss

LCP	liquid crystal polymer
LTCC	low-temperature co-fired ceramic
MCM	multichip module
MEMS	micro-electro-mechanical-system
μm	micron = 10^{-6} meter
MIMO	multiple-input multiple-output
mm	millimeter = 10^{-3} meter
MMIC	monolithic microwave integrated circuit
MOM	method of moments
nH	nano henries = 10^{-9} henries
PCS	personal communication services
PECVD	plasma-enhanced chemical vapor deposition
pF	pico farads = 10^{-12} farads
ppm	parts per million
Q_e	external quality factor
Q_L	loaded quality factor
Q_u	unloaded quality factor
RIE	reactive ion etch
RF	radio-frequency
RLL	return loss level
Si	silicon
SiGe	silicon germanium
SiP	system-in-a-package
SIR	stepped impedance resonator
SoC	system-on-a-chip
SOLT	short, open, load, and thru
SoP	system-on-a-package
STS	Surface Technology Systems
tan δ	loss tangent

Ti	titanium
TM	transverse magnetic
T/R	transmit/receive
TRL	through-reflect-line
WLAN	wireless local area network

SUMMARY

The objective of this thesis is to realize high-linearity, five-bit High-Low pass phase shifters for use in a monolithic transmit/recieve (T/R) module at X-band (8.5–10.5 GHz). The contributions of this research are a comprehensive analysis of the sources of phase error associated with the high-low pass phase shifter topology, a wide-band near-hermetic packaging method for Radio Frequency (RF) Micro Electromechanical System (MEMS) switches, and high performance phase shifters implemented on high resistivity silicon with packaged RF MEMS switches and on SiGe with active switches.

The first few sections focus on developing a greater understanding of the present shortcomings of the High-pass/Low-pass topology. This includes a comprehensive analysis of error sources in monolithic microwave phase shifters because of device size limitations, inductor parasitics, loading effects, and non-ideal switches. Each component utilized in the implementation of a monolithic high-low pass phase shifter is analyzed, and its influence on phase behavior shown in detail, with an emphasis on the net impact on absolute phase variation. The design of the individual phase shifter filter sections, and the influence of bit ordering on overall performance is also addressed. An X-band five-bit phase shifter fabricated in a 200 GHz SiGe HBT BiCMOS technology platform is used to validate the analysis and design methodology. This SiGe phase shifter targets incorporation into a single-chip T/R module forming a system-on-a-chip (SoC).

The second research topic investigates spinel magnetic nanoparticle films, and their effectiveness in reducing the physical size of transmission lines. The signal transmission properties of phase lines treated with nanoparticle thin films is examined, providing the potential for significant size reduction in both delay line and High-pass/Low-pass phase topologies.

Next, a wide-band low-loss near-hermetic packaging technique for RF MEMS devices is presented. This is created to be compatible with standard IC fabrication techniques and uses

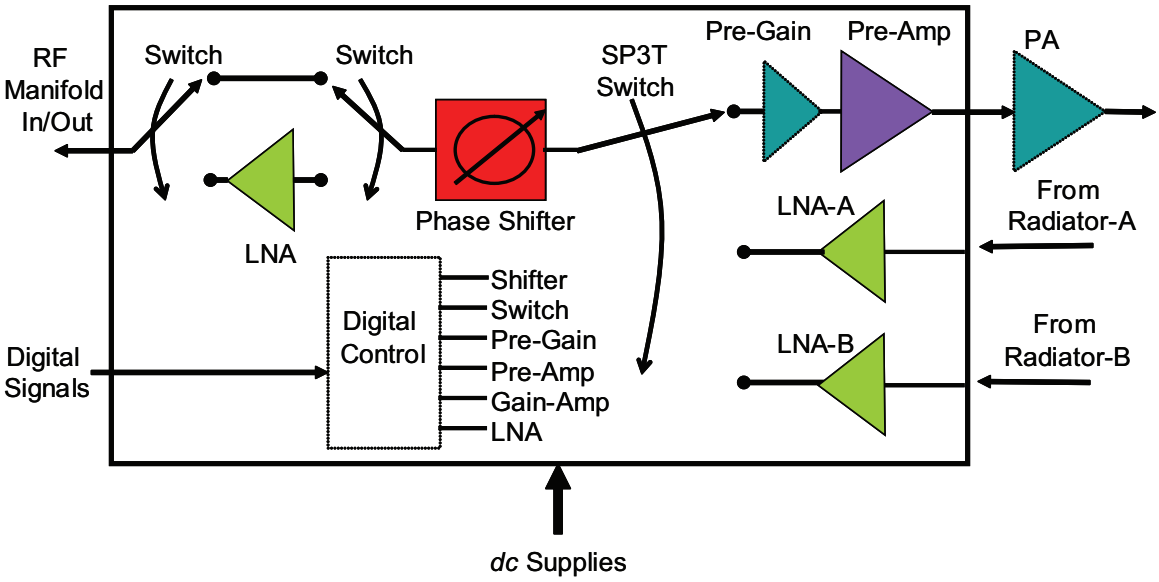

Figure 1: A conceptualized T/R module showing the relationship of the phase shifter to integrated sub-systems.

a low temperature thermal compression bonding method that avoids plastic deformations of the MEMS membrane. An alternative organic polymer based packaging solution is also addressed.

Finally, a system-on-a-package (SoP) approach is examined that will utilize packaged RF MEMS switches on high resistivity silicon to maintain the performance of the SiGe phase shifter with much lower loss than the HBT- and MOS-based SiGe phase shifters. Careful attention is given to the phase performance as it has a direct impact on the beam-steering capabilities of a phased array. The phase shifter utilizes the largest die area of any subsystem in the module, hence small size will be an additional goal. A block diagram showing the relationship of the phase shifter to the T/R module is shown in Fig. 1.

CHAPTER I

INTRODUCTION

Since its introduction in World War I, radar has continued to evolve into increasingly complex and multi-functional systems. Current radar research and development continues to be driven in large part by military applications such as surface radar, missile guidance, and satellite-based radar, but civilian applications such as automotive radar, radio astronomy and weather radar are finding new uses and requirements for radar technology. All present research builds upon work done over the last century, primarily the breakthroughs on radar technology achieved after the first World War.

In 1937, Fris developed an antenna array that provided an improvement in signal-to-noise ratio (SNR) by increasing the directivity of the main lobe [17]. Although this array was mechanically tuned, it was the first step toward the phased arrays seen today. Using multiple antennas with specific spacing and orientation (such as dipoles placed in parallel 1/4 λ apart), constructive and destructive interference could be used to control the direction of the maximum power wavefront (Fig. 2). This was done by manipulating the phase of each radiating element. With a grid of radiating elements, this maximum power wavefront could be aimed at any point visible to the radar, typically a cone shape with an interior angle of about 90-120°. Increasing the number of elements in the array would increase the directivity, providing an increase in resolution. At a set distance from the radar, higher resolution would provide greater discrimination between multiple targets in close proximity.

Near the end of World War II, the technology to electronically steer the array was developed [74]. The key advantage of the phased array over conventional radar is the ability to control the beam without the use of mechanical systems. This not only increased the system reliability, but also provided other significant benefits, such as

- Increased data rates

- Instantaneous beam positioning
- Elimination of mechanical errors
- Multi-mode operation
- Multi-target capability

A drawback of phased arrays over conventional radar is that its resolution is dependant on the number of radiating elements. In addition to a large number of antennas, T/R modules are required to control the signal flow, amplification, and phase. These modules were made up of sub-systems on separate chips, generally GaAs or InP MMICs for the PA and LNA with separate p-i-n diode devices for switches and phase shifters. Many implementations for these modules have been examined in the past decade [1, 18, 22, 27, 39, 44]. However, their size and cost continue to remain a significant problem to the development of lower cost high-performance phased arrays.

In the past few years, there has been a focused effort on integrating large parts of the T/R module into a single chip. This system-on-a-chip (SoC) approach provided the desired attributes of size and cost, but introduced many additional problems. For better digital and analog integration, the high power capabilities of GaAs were exchanged for the versatility of silicon. The large footprint of the phase shifter and limited switch performance deemed many phase shifting topologies unfeasible. Integration issues increased in complexity with the close proximity of devices such as the PA and LNA. However, the advantages of a single-chip T/R module greatly outweigh the design challenges.

Recently, SiGe has emerged as the optimal choice for SoC phased arrays [31]. While keeping the integration ease of silicon, SiGe provides a number of benefits over silicon:

- Reduced noise figure (NF) and phase noise
- Increased frequency range and device matching capabilities
- Higher breakdown voltage and transconductance

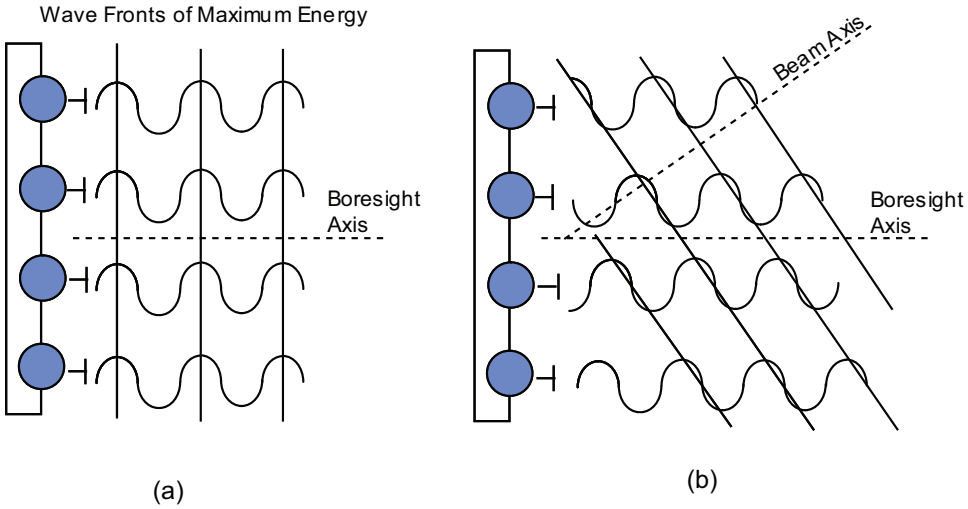

Figure 2: A simple phased array showing beam axis for when (a) all elements are radiating in phase, and (b) each element is shifted in phase by a specific amount.

- Enhanced temperature performance (a negative current gain across temperature causes increased gain and improved noise performance with lower temperature)

1.1 Phase Shifters for Radar Applications

The phase shifter is at the very heart of phased array radar, and beam-steering performance is directly tied to the phase performance of the phase shifter. Generally, the phase performance of a phase shifter is related to its insertion loss. When phase error is extremely important (i.e., military radar), insertion loss can be overcome with additional amplification for an increase in cost and power consumption. For systems where phase error is less important than power consumption (i.e., automotive radar), the trade-off can again be made.

For operating frequencies above a few GHz, there are only four main types of digital phase shifters: switched line, reflection, loaded line, and high-low pass. Some phase shifters in the literature mix these types, but each bit follows a single topology.

1.1.1 Switched Line Phase Shifter

The switched line phase shifter is the most direct topology for a phase shifter (Fig. 3a). It switches between line l_1 and l_2, providing a time delay determined by $\Delta l = l_1 - l_2$. In its

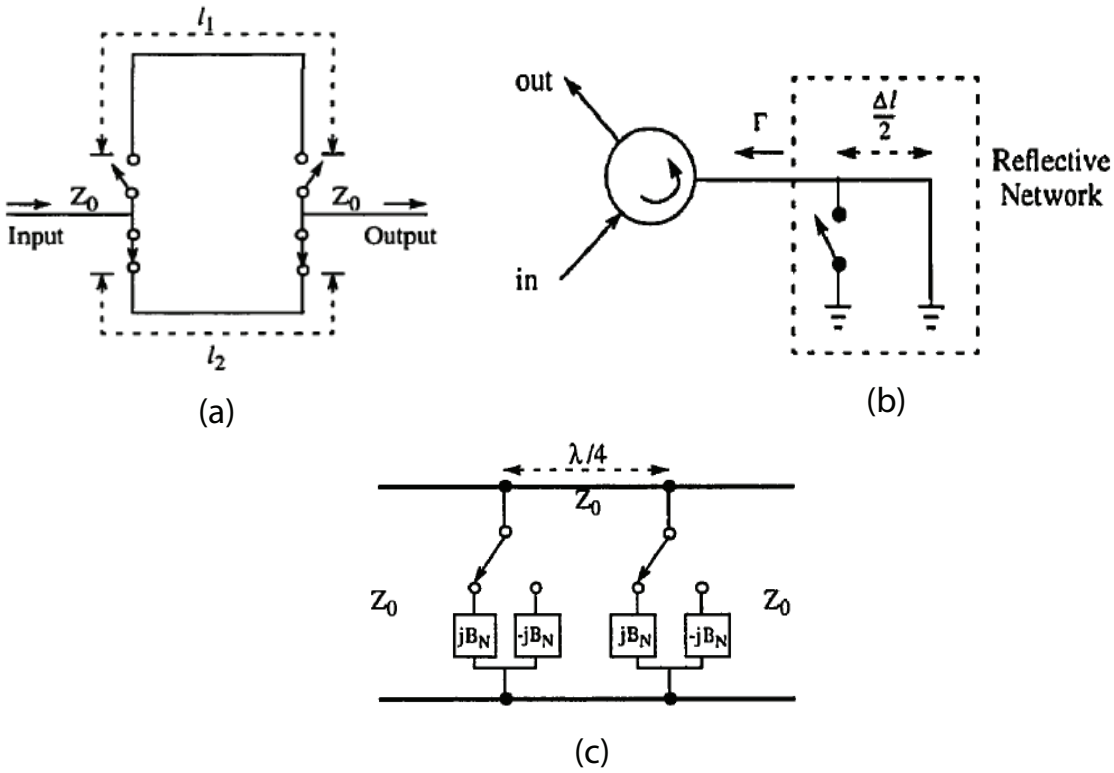

Figure 3: a) A switched line phase shifter. b) A reflection phase shifter. c) A loaded-line phase shifter. Taken from [19].

common form, each bit will have a reference path l_2 with an alternative path l_1 which is longer in length such that $\Delta\phi = 2\pi\Delta l/\lambda$.

Phase errors are easily introduced by coupling between lines or changes in line characteristic impedance (a common problem with curved sections) and path leakage from non-ideal switch isolation. The largest drawback to this topology is its reliance on long transmission lines, which for on-chip solutions provides extremely high loss with non-uniformity of loss across different phase combinations, and significant chip real estate.

An alternative topology has been recently examined in the literature [35] to dramatically reduce size and path length problems. However, the severe bandwidth limitations introduced by the 100 Ω characteristic impedance lines make this an impractical method for broad-band applications.

1.1.2 Reflection Phase Shifter

The reflection phase shifter is a popular variation of the switched-line topology (Fig. 3b). This utilizes a short circuit at the end of a transmission line with another short that can be activated at a distance of $\Delta l/2$ before the end short. A signal going through the input of the circulator will then either be reflected at the activated short or end short, and return to the output of the circulator.

An advantage of this topology over the switched line is that a single line may be used for multiple desired phase shifts, with switches placed along the transmission line at the proper locations. However, use in an on-chip phase shifter is difficult as the phase performance is quickly degraded by non-ideal shorts and circulators. This method, however, is well suited for MEMS applications where MEMS can provide open and short behavior much closer to ideal [40].

1.1.3 Loaded Line Phase Shifter

The loaded-line phase shifter (Fig. 3c) differs from the previous two by manipulating characteristics of the transmission line opposed to changing the physical length of the signal path. This can result in smaller die areas than the previous topologies, but its reliance on the $1/4\lambda$ section produces a band-limited response. [26]

1.1.4 High-Low Pass Phase Shifter

The High-Low Pass phase shifter (Fig. 4) was first introduced over 30 years ago [51], with the first detailed analysis soon after in [19]. The original advantage of this shifter was its superior power and phase bandwidth capabilities.

The high-low pass phase shifter functions by taking the difference between the phase from the high pass filter path and the low pass filter path of a particular bit. Each individual bit will have independent high and low pass paths, with SPDT switches on both sides of the bit (Fig. 4). These filters are specifically designed for both very small rejection in the band of operation and a linear phase response, which is set to either advance or delay the phase by half the desired amount, depending on which path is selected.

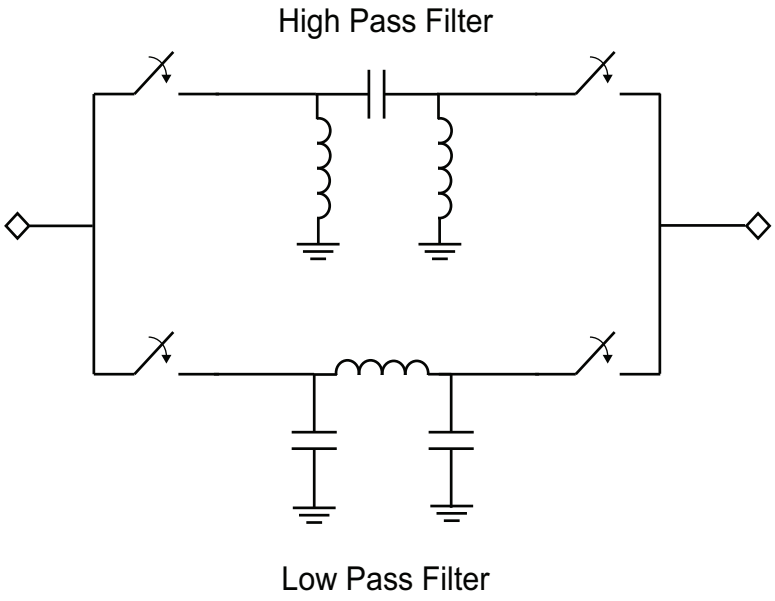

Figure 4: A single bit in a switched line phase shifter.

Because this topology does not depend on specific transmission line lengths, a constant phase shift over a bandwidth of more than an octave can be achieved. This is possible because the phase response of both the high and low pass paths behaves similarly when moving away from the center frequency, causing a constant difference in phase between the two paths.

1.2 High-Low Pass Phase Shifters on SiGe

In the past five years, there has been a renewed interest in the use of the high-low pass shifter topology, particularly in SiGe IC design platforms targeting monolithic transmit/receive (T/R) module applications for phased array radar [9, 70]. From simple bit topologies with p-i-n diode switches [66], to more complicated designs [24], the high-low pass phase shifter has been found to be an ideal architecture because of its small size, flat phase response over a broad band, and its ability to cancel out phase effects from switches and routing schemes.

However, inherent device limitations in silicon-based (e.g., SiGe) monolithic design approaches make achieving optimal phase performance difficult. Only a narrow range of inductor and capacitor values may be fabricated, complicating bit designs for a given band of

operation. The inductors pose additional challenges because of their inherently higher parasitics in silicon technology, resulting in lower Q and self-resonance frequencies. Single-pole double-throw (SPDT) switch performance may also increase the phase variation associated with a given shifter. The phase performance of a single bit can additionally influence the phase of adjacent bits, leading to integration challenges and a degradation of overall shifter performance.

A survey of the current state of the art for monolithic high-low pass phase shifters is shown in Table 1. The University of Michigan demonstrated a phase shifter with gain and the smallest size [24]. However, this gain is achieved with an additional LNA and the size reduction is due to tunable operation. This produced large phase errors and linearity unsuitable for a phased array T/R module application. Hittite demonstrated a phase shifter with good phase performance and very low loss using an mHEMT process [32], but linearity and compression performance were not revealed. The mHEMT process is much more expensive than SiGe, closer to the cost of GaAs with similar performance to InP. Raytheon produced a phase shifter on SiGe with p-i-n diodes [66] that provided good linearity and compression, but phase error was large. Two phase shifters designed by the author and Jonathan Comeau are also shown [10, 11], which exhibit the best phase performance, linearity and compression. However, these phase shifters also show the highest loss.

The bulk of this loss occurs in the switches, with two switches required for every bit used. It is unlikely the loss for a five-bit phase shifter can be reduced significantly using technology available on the SiGe process. However, it would be possible to develop MEMS switches via a post-processing technique that would replace the lossy MOS and HBT devices with very low loss and even higher linearity MEMS switches.

1.3 RF MEMS Switch Development

RF MEMS switches have shown great potential for the development of low-loss, low-power and low-cost reconfigurable and smart antenna systems on-chip or on-package by introducing revolutionary phase shifter circuits, impedance matching networks, and switching matrices for MIMO systems [52,57]. It is widely recognized that the advantages offered by the MEMS

Table 1: Comparison of current competitive High-Low Pass phase shifters

	ϕ Error	Loss (dB)	Area (mm^2)	P_{1dB} (dB)	IIP3 (dB)	Note
Raytheon	25°	14	14	3	17	p-i-n
U. Michigan	20°	3.7*	1.1	-27.3	-17.3	Tunable
Hittite	10°	6.5	1.7	NR**	NR**	mHEMT
GEDC	7°	12.3	9.6	5.7	20	HBT
GEDC	5°	17.2	8.1	8.6	21	MOS

* 3.7 gain, design incorporates LNA, ** NR: Not Reported. Sources: [10, 11, 24, 32, 66]

switch technology cannot be achieved without an appropriate package that will shield and protect the switch, as well as an interconnect technology that will allow for easy RF and DC signal transition in and out of the package.

Low-loss, wide-bandwidth hermetic packages are therefore essential for practical high-performance RF MEMS devices. Among the many problems faced with package design, the interconnect is at the core of RF performance. For an interconnect to function largely independent of frequency, the interconnect itself as well as the surrounding transition region must act as a transmission line. Previous attempts to lessen the effects of the bonding materials on transmission line behavior of the interconnect focused on using BCB [68] or localized aluminum/silicon-glass bonding [76] with polysilicon for the interconnect, which is lossy for RF applications. Alternatively, simple techniques such as thermal compression bonding require a metal ring to fully enclose the packaged region. This complicates interconnect design, as the interconnects must access the internal region of the package either by buried layers or from the other side of the substrate through vias [2], [42]. Proper geometries for high-performance transmission lines are difficult to control under these circumstances, and may also be costly in terms of fabrication.

If a viable and cost-effective packaging solution is found, a high-low pass phase shifter SoC with very low loss, excellent phase performance, linearity, and compression is possible.

CHAPTER II

TRANSMISSION LINES ON SIGE

As few as ten years ago, studies of transmission lines in conventional silicon IC technology were virtually nonexistent because of the poor intrinsic performance of the requisite transistor building blocks. This scenario has changed radically, however, with the emergence of bandgap-engineered SiGe HBT technology as a viable competitor in the microwave and millimeter-wave arena.

Today, SiGe HBTs with peak f_T/f_{max} values above 200 GHz exist in commercial foundries, and record values of f_T of 350 GHz have been reported [58], making the emergence of viable, low-cost, integrated microwave and millimeter-wave systems up to 100 GHz using conventional Si IC manufacturing a real possibility. Clearly, the eventual success of such systems requires not only active components, but also schemes for the on-chip interconnection of the active circuitry. One such potential solution is to use a coplanar waveguide structure on high resistivity silicon, as was reported in [55]. Such a substrate, however, is not traditionally available in commercially available (low-cost) SiGe processes, and if it is, definitely comes only at an undesirable cost. An alternate, potential transmission line configuration is that of the Thin Film Microstrip (TFMS).

2.1 Thin Film Microstrip Line

On a standard SiGe process, the signal line and the ground can be selected as the topmost and lowest routing metals available in the process, respectively, as can be seen in Fig. 5. Such a configuration was explored in [54]; however, the use of polymide dielectrics is also not commercially available as a dielectric in foundry processes and thus they are undesirable from a cost perspective. Additional work ([21], [5], and [71]) also explored the use of commercially available processes, but only provided measured data up to a maximum of 40 GHz.

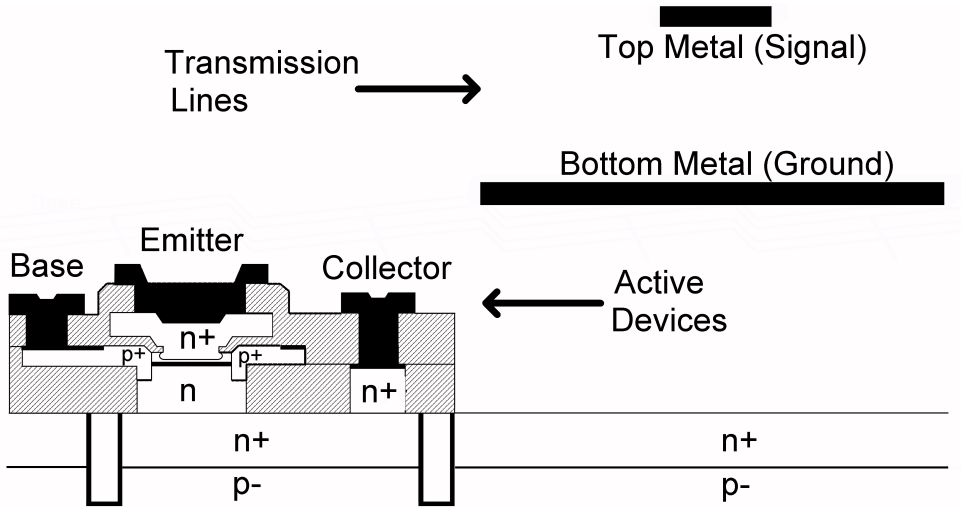

Figure 5: Representation of active devices and on silicon transmission lines. Drawing not to scale.

TFMS lines were fabricated and measured on a commercially available SiGe HBT process without additional post-fabrication processing while maintaining strict adherence to IC design rules. Such lines required slotted ground planes to meet the design rule criteria. The measured data on these lines is presented for the first time to 110 GHz.

2.2 Design and Measurement

TFMS lines were designed that provided a nominal 50 Ω characteristic impedance on the four-layer metal process from the commercial SiGe HBT BiCMOS process used. The top layer was used as the signal line, with the bottom layer used as ground. Process design rules mandated that wide metal, such as a ground plane, have periodic slots placed in it for planarity at higher physical levels. Thus, slots were placed in the ground plane with dimensions of 10 μm x 90 μm with metal runs of 20 μm in between, as can be seen in Fig. 6. Because of the narrow separation between the signal and ground, nominally 3.24 μm, a very narrow line width of 7 μm wide had to be used for the signal trace. This line was transitioned to a grounded CPW structure through a taper to facilitate probing.

Characterization of the lines was performed from 20 to 110 GHz using an Agilent 8510C vector network analyzer. Line loss was calculated through the use of Thru-Reflect-Line (TRL) structures that were placed on the design (see Fig. 7). These structures consisted

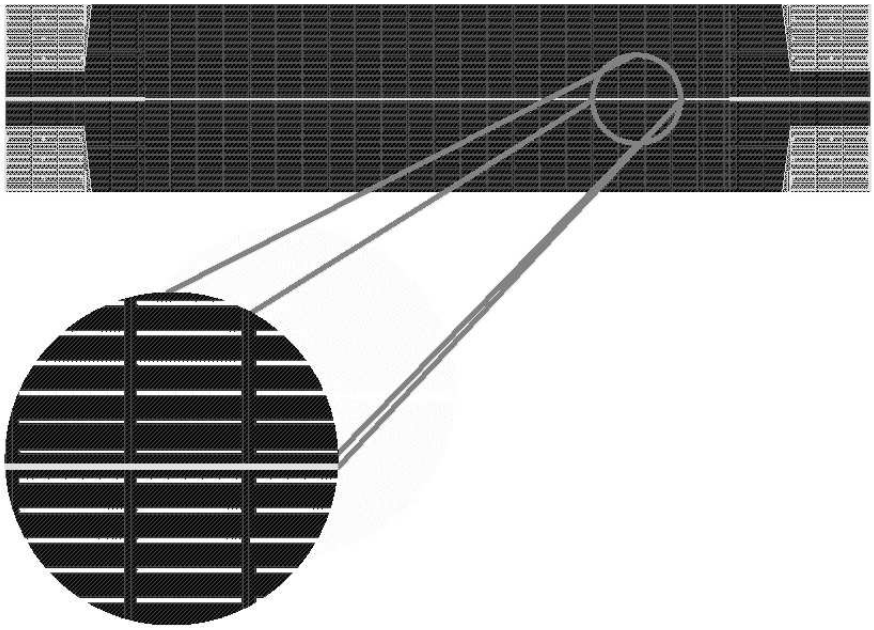

Figure 6: Layout of the transmission lines with the inset showing the ground plane slots.

of an "open" and a "short" of the CPW with a taper structure, as well as line lengths of 550, 1100, 2200, and 4400 μm. The de-embedding software used was the MULTICAL [43] software provided by NIST. This software allowed for reflections and losses of the transitioning CPW structures to be calibrated out, leaving only the TFMS signal trace.

2.3 Discussion

The measured loss of the TMFS line, shown in Fig. 8a, is given in dB/cm as well as dB/λ_g. While the loss per cm is high for the millimeter frequency bands that are interesting to the integration of transmission line structures on SiGe processes, the loss per guided wavelength remains practical for typical microwave designs. The integration on SiGe would also allow for transistor amplification to overcome this loss.

The measured loss of the CPW line, shown in Fig. 8b, is also given in dB/cm and dB/λ_g. Unlike the TFMS line, CPW structures show little promise in this commercial process for practical design. This large loss is due primarily to the low-resistivity silicon used as the substrate. Conductor-backed CPW is not an option, as the thin 3.24 μm oxide layer separating the metal layers would require an extremely narrow center conductor to

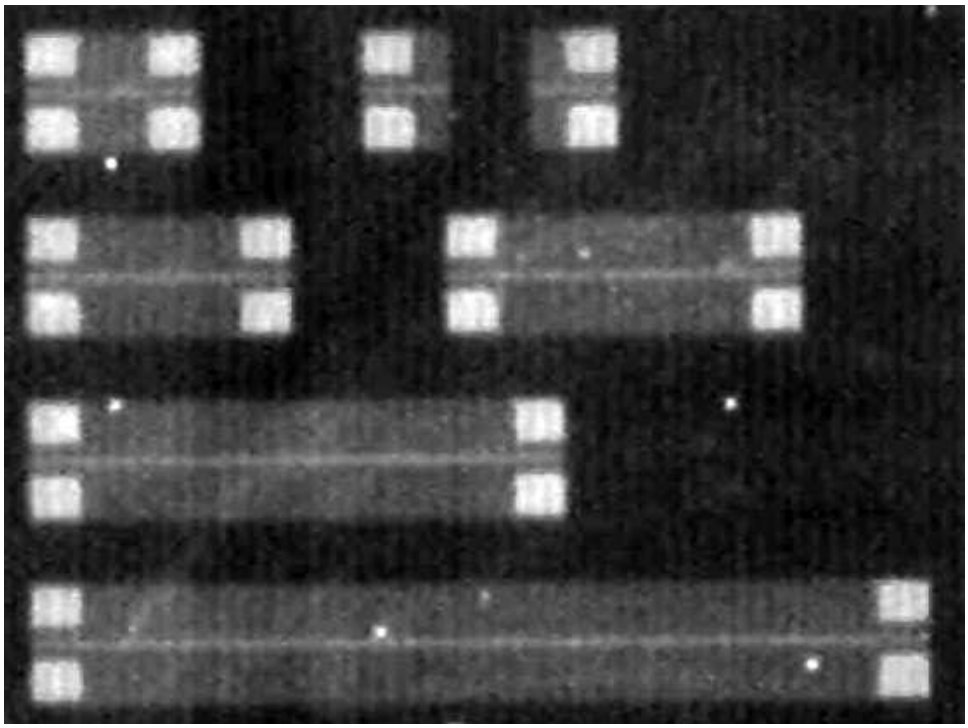

Figure 7: Die photo of TRL structures of TFMS lines on wafer.

keep the microstrip mode from dominating, and very large losses would again result.

The measured reflection for both the TFMS and CPW lines is shown in Fig. 9a. Low reflections indicate that the lines were well matched to 50 Ω, so the attenuation is dictated by either losses in the metal or the substrate, or by radiation. The fraction of the total power lost through these effects is shown for each line type in the power loss budget analysis in Fig. 9b. This value is calculated by 1 - $|S_{11}|^2$ - $|S_{21}|^2$, and shows that between 30 and 70 percent of the power is lost in the TFMS line, and nearly all of the power is lost in the CPW line.

2.4 Summary

Measurements of CPW and TFMS lines on a commercially available SiGe HBT BiCMOS technology process up to 110 GHz have been shown. Because of standard substrate resistivities, it is clear that unshielded CPW lines are not viable for this process. A conductor-backed CPW approach is difficult, as the separation between the metal layers is too small. This would require a center conductor smaller than that which is allowed by design rules

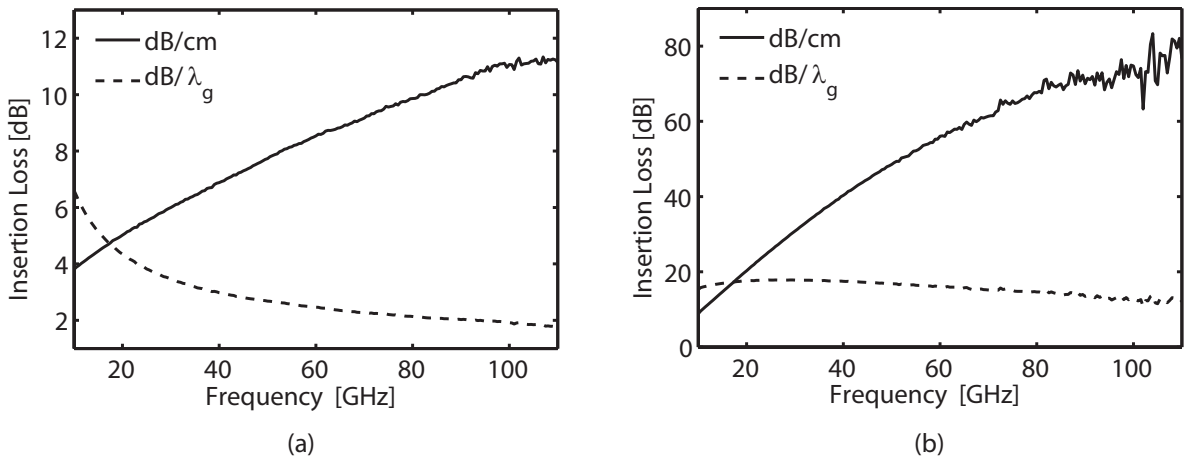

Figure 8: Measured attenuation of the lines in dB/cm and dB/λ_g: (a) microstrip, (b) CPW.

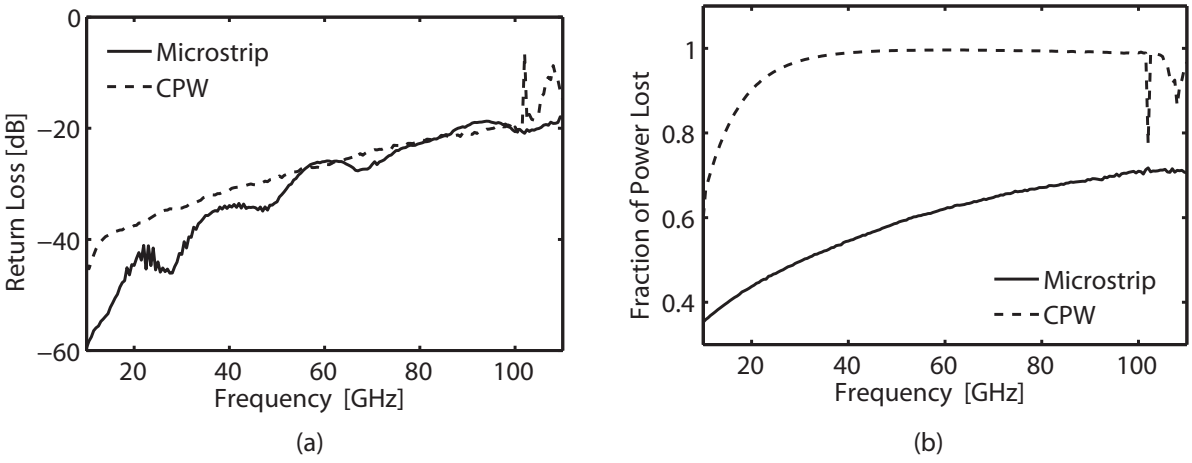

Figure 9: (a) Measured reflection of microstrip and CPW lines. (b) Power loss budget analysis. The fraction of power that is not reflected or transmitted.

and would also greatly increase the loss. The TFMS approach shows potential for emerging MMIC and millimeter-wave applications.

However, the large line lengths required for phase shifters using the loaded-line or reflection topologies would create extremely large system losses. TFMS lines could be used for short signal routing paths, but it is clear that phase shifting topologies dependent on sections of transmission lines are not viable at X-band.

CHAPTER III

SOURCES OF ERROR AND DESIGN CONSIDERATIONS FOR THE HIGH-LOW PASS PHASE SHIFTER

The high-low pass phase shifter functions by taking the difference between the phase from the high-pass filter path and the low-pass filter path of a particular bit. Figure 10a shows a block diagram of such a 5-bit phase shifter, with a typical schematic of the first bit and surrounding switches shown in Fig. 10b. These filters are specifically designed for both very small rejection in the band of operation and a linear phase response, which is set to either advance or delay the phase by half the desired amount, depending on which path is selected.

Each individual bit will have independent high- and low-pass paths, with SPDT switches on both sides of the bit. The functionality and impact of non-idealities for each component will be examined individually, starting with the high-pass and low-pass sections at the heart of the shifter (Fig. 24).

3.1 Three-element Paths

As shown in [19], the transmission phase for the three-element case of Fig. 24 switched in the low-pass state is given by

$$\phi = tan^{-1}\left[-\frac{X_N + 2B_N - X_N B_N^2}{2(1 - B_N X_N)}\right] \tag{1}$$

This phase response is shown in Fig. 12a for a range of B_N and X_N. When switching between low- and high-pass paths, both B_N and X_N change signs. Because the phase will now change only in sign, the phase shift $\Delta\phi$ caused by switching between the low- and high-pass paths is doubled.

By assuming the phase shifter to be loss-less, B_N and X_N can then be solved in terms of $\Delta\phi$, giving

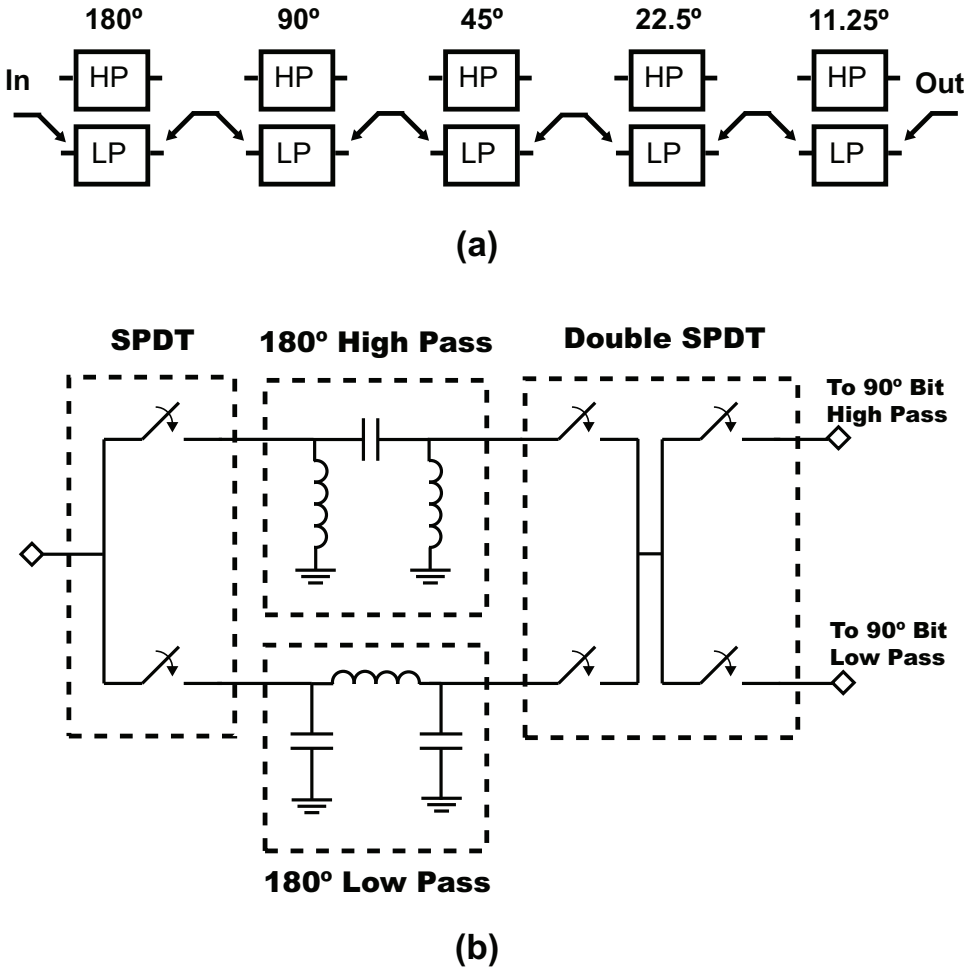

Figure 10: a) Block diagram of a 5-bit high-low pass phase shifter. b) A generalized schematic of the first SPDT switch, the filter sections for the initial bit, and the back-to-back SPDT switches that separate adjacent bits.

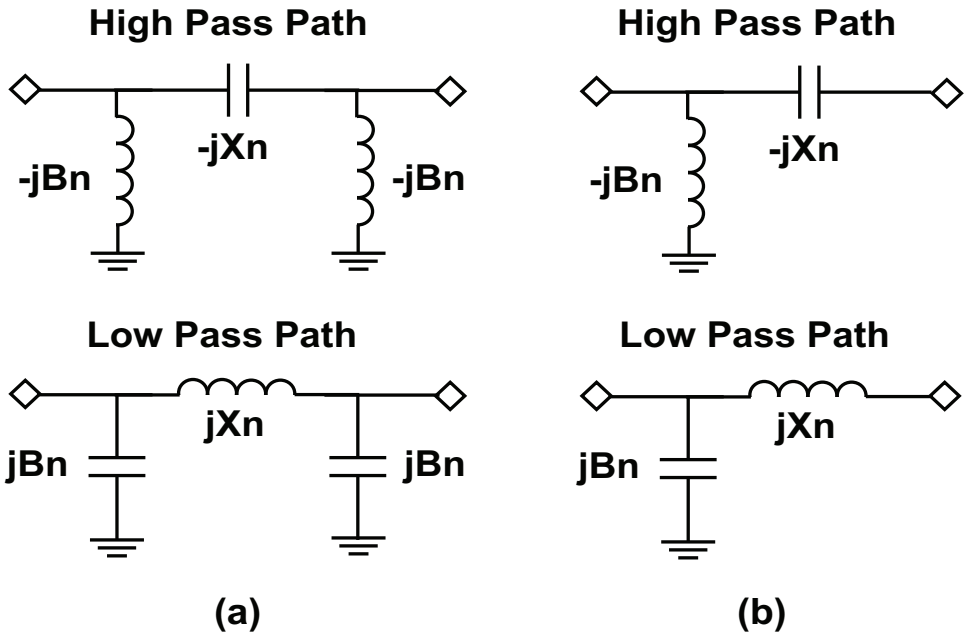

Figure 11: a) The three-element high-pass low-pass filter sections with $B_N = tan(\Delta\phi/4)$ and $X_N = sin(\Delta\phi/2)$. b) The two-element filter sections with $B_N = tan(\Delta\phi/2)$ and $X_N = sin(\Delta\phi/2)cos(\Delta\phi/2)$.

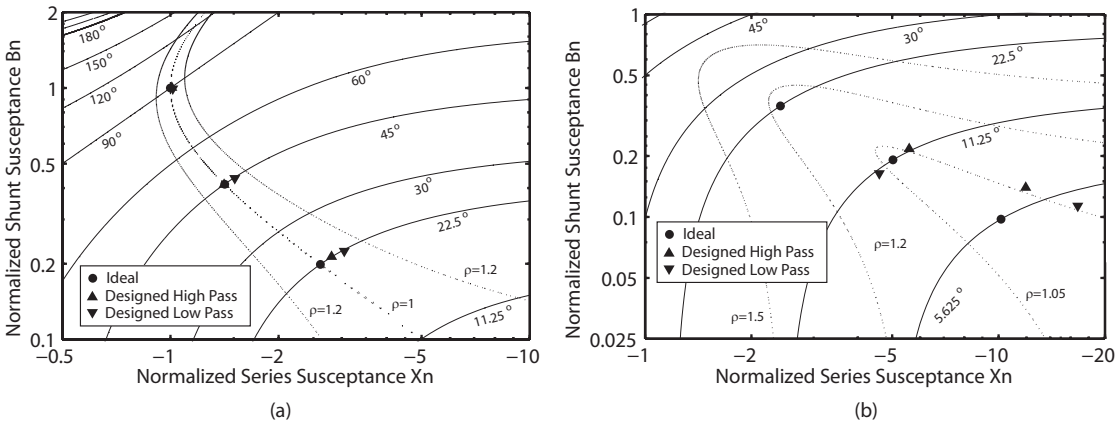

Figure 12: Phase shift of lumped-element low-pass pi-section phase-shift paths. Values calculated from (2) and (3) are marked with filled circles. Values used in our designed phase shifter are marked with an upward pointing triangle for the high-pass section and downward pointing triangle for the low-pass section. (a) Three elements in path, (b) Two elements in path.

Table 2: Values for ideal three-element bits at 9.5 GHz.

	High Pass		**Low Pass**		
Shift	C (pF)	L (nH)	C (pF)	L (nH)	S_{11}^*
180°	.3351	.8377	.3351	.8377	-9 dB
90°	.4739	2.0223	.1388	.5923	-20 dB
45°	.8756	4.2112	.0667	.3206	-27 dB
22.5°	1.718	8.505	.0333	.1634	-36 dB
11.25°	3.418	17.051	.0165	.0821	-45 dB

*__Worst S_{11} in 8.5-10.5 GHz__

$$B_N = tan\left(\frac{\Delta\phi}{4}\right) \tag{2}$$

and

$$X_N = sin\left(\frac{\Delta\phi}{2}\right). \tag{3}$$

Using these equations to generate values for an X-band shifter (Table 2), we find that the values required for the 22.5° and 11.25° bits are impractical for use in most commercial silicon-based processes since they are either extremely large or small (i.e. C $<$ 20 fF, L $>$ 10 nH). If a T-section is used instead of a pi, X_N and B_N would be exchanged (2 and 3). This changes which filter section (high pass or low pass) contains large or small values, providing no advantage to requisite device sizes or resultant phase performance.

3.2 Two-element Paths

Reducing the high- and low-pass filter sections to two elements allows for component values (at X-band) more compatible with commercial silicon-based fabrication limitations. In this case, (1) becomes

$$\phi = tan^{-1}\left[-\frac{X_N + B_N}{2 - B_N X_N}\right] \tag{4}$$

This phase response is shown in Fig. 12b for a range of B_N and X_N, and again the

phase shift ($\Delta\phi$) caused by switching between low pass and high pass is double the shift from each path individually.

In this two-element case, and again assuming the shifter to be loss-less, we find that

$$B_N = tan\left(\frac{\Delta\phi}{2}\right) \tag{5}$$

and

$$X_N = sin\left(\frac{\Delta\phi}{2}\right) cos\left(\frac{\Delta\phi}{2}\right) \tag{6}$$

Using these equations to generate values for an X-band shifter (Table 3), we find that the values required for the 22.5° and 11.25° bits are much more reasonable than for the three-element case. However, in the two-element case, a minimum $VSWR$ penalty for an increase in desired phase shift occurs. For the 22.5° and 11.25° bits this degradation is negligible, however.

While these component values are more compatible with commercial silicon-based fabrication processes, it is possible to make a trade-off between component values and the reflection and phase performance. These designed values can be seen in Table 4 and are also shown in Fig. 12, with upward arrows marking the high-pass values and downward arrows marking the low-pass values. The differences between ideal and designed values become more pronounced as the desired shift decreases. The worst case is the 11.25° bit, where the individual paths no longer produce 5.625° of phase shift. Here, the high-pass and low-pass sections provide 6.35° and -4.9° of phase shift, respectively, giving the total desired 11.25°. While moving away from the optimal design points for these lower shift value bits reduces the $VSWR$ and bandwidth of acceptable phase performance, they are still generally as well behaved as the higher shift value ideal bits, and pose no serious problems for typical bandwidth requirements in X-band radar systems ($8 - 12GHz$).

3.3 Effects of Inductor Parasitics

While both capacitors and inductors in monolithic silicon-based technologies are non-ideal, the parasitics from inductors are typically much more pronounced. The ideal inductors in

Table 3: Values for ideal two-element bits at 9.5 GHz.

	High Pass		**Low Pass**		
Shift	C (pF)	L (nH)	C (pF)	L (nH)	S_{11}^*
45°	.8089	2.369	.1185	.3470	-10 dB
22.5°	1.684	4.378	.0641	.1667	-16 dB
11.25°	3.402	8.587	.0327	.0825	-22 dB

***Worst** S_{11} **in 8.5-10.5** GHz

Table 4: Values for designed bits for 9.5 GHz.

	High Pass		**Low Pass**		
Shift	C (pF)	L (nH)	C (pF)	L (nH)	S_{11}^*
[3]180°	.3400	.8429	.3360	.8304	-10 dB
[3]90°	.5061	1.915	.1382	.5941	-13 dB
[3]45°	1.021	3.726	.0715	.2984	-13 dB
[2]22.5°	1.872	3.863	.0550	.1821	-14 dB
[2]11.25°	4.000	6.000	.0380	.0500	-15 dB

***Worst** S_{11} **in 8.5-10.5** GHz**,** [2]**2-element bits,** [3]**3-element bits**

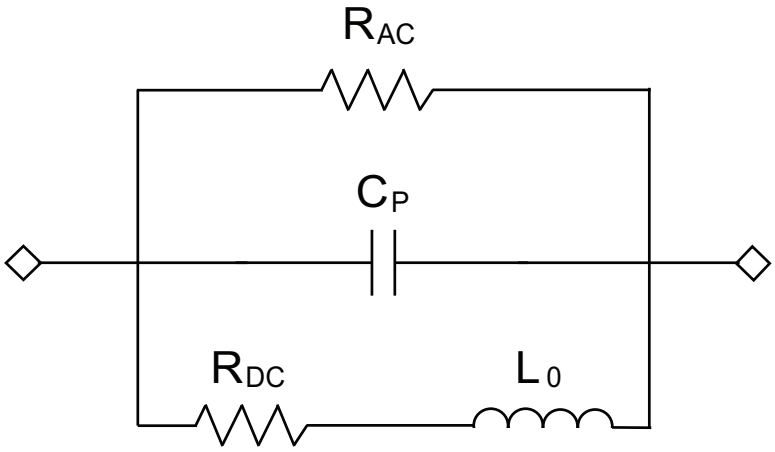

Figure 13: A simple inductor model.

Fig. 24 will be replaced with a simple model, as shown in Fig. 13. This will allow us to examine the effects of magnetic loss, *DC* resistance, and self-resonance on phase shifter performance.

Self-resonance is modeled with a capacitor C_P in parallel to the series inductor and resistor [50]. The value of this capacitance is derived from the equation

$$C_P = \frac{1}{(w_{res})^2 L_0} \tag{7}$$

Inductor Q is modeled with R_{DC} and R_{AC}, accounting for *DC* resistive loss and magnetic and skin effect losses, respectively.

$$Q = \frac{w_{res} L_0 R_{AC}}{(w_{res} L_0)^2 + R_{DC}(R_{AC} + R_{DC})} \tag{8}$$

When we look at the equivalent impedance (normalized for a given frequency) of this inductor model, we find that

$$j\widetilde{X_N} = \frac{R'_P C'_P R'_{DC} + j(R'_P C'_P L'_0)}{C'_P(R'_{DC} + R'_P) - R'_P L'_0 + j(R'_P R'_{DC} + C'_P L'_0)} \tag{9}$$

where C'_P, R'_{DC}, R'_P, and L'_0 are the normalized impedances of their corresponding values. It is now important to note that the phase shift of the high-pass and low-pass paths will behave differently. To simplify the analysis, each non-ideal behavior is examined independently.

3.3.1 Effects from Series Resistance

First looking only at series resistance, and temporarily ignoring the other parasitics, (9) can be simplified to

$$j\widetilde{X_N}_{,w_{res}=\infty} = R'_{DC} + jL'_0 \tag{10}$$

The transmission phase for the low-pass path is

$$\phi_{lp} = tan^{-1}\left[-\frac{BR^2 + 2BR + B + 2L - BL^2}{2(R+1)(1-BL)}\right] \tag{11}$$

where $R = R'_{DC}$ and $L = L'_0$, and the transmission phase for the high-pass path is

$$\phi_{hp} = tan^{-1}\left[-\frac{2RX - LX^2 + 2X + L}{R(1-X^2) + 2(1-LX)}\right]. \tag{12}$$

An increase in series resistance R_{DC} causes an insignificant decrease in $\Delta\phi$, but will increase the phase variation over a set band of operation by shifting the center frequency of the response higher. This can be seen in Fig. 14a, with phase responses for $R_{DC} = 0, 5$ and 10 Ω. While phase effects from resistive losses were negligible in the earlier discrete cases, the thin metal layers on commercial silicon-based processes easily contribute a few ohms of resistance in the best cases and an even more pronounced effect where internal layers or large inductor values are used.

This shift in the center of the phase response from R_{DC} can be seen in Fig. 14b, showing three-element bits with solid lines and two-element bits with dashed lines. For the three-element bits, the frequency of the local minimum steadily increases, with very little difference in behavior between the bits. The two-element case also has a common functional form among the bits, but there is an overall shift upward for higher shift-value bits. This effect, along with the aforementioned $VSWR$ penalty, is another reason to reduce the number of elements in a bit only when it is necessary to keep passive device sizes reasonable. For a set band of $0.8w - 1.2w$ the relative phase error grows steadily as R_{DC} is increased, as shown in Fig. 15. These phase errors will compound for a multi-bit phase shifter.

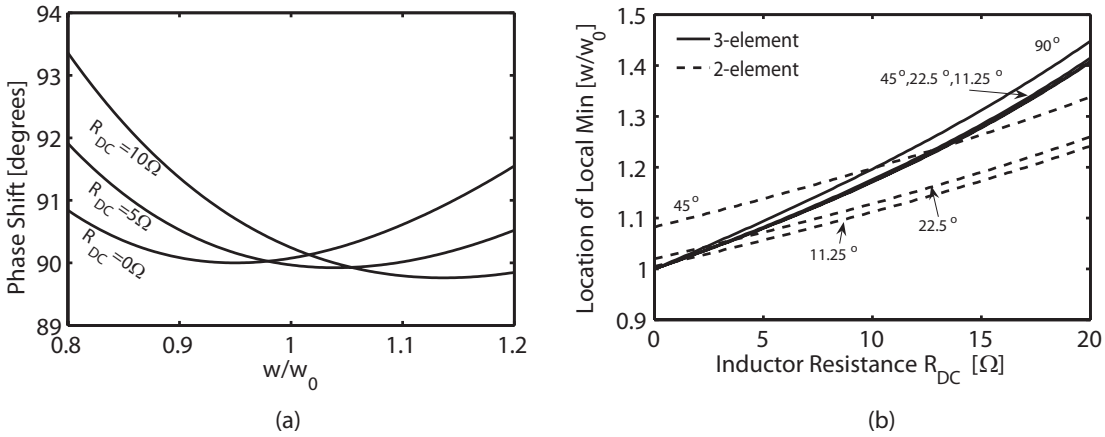

Figure 14: (a) Phase shift produced using inductors with series resistance $R_{DC} = 0, 5$ and 10 Ω. (b) Location of local minimum with swept R_{DC}.

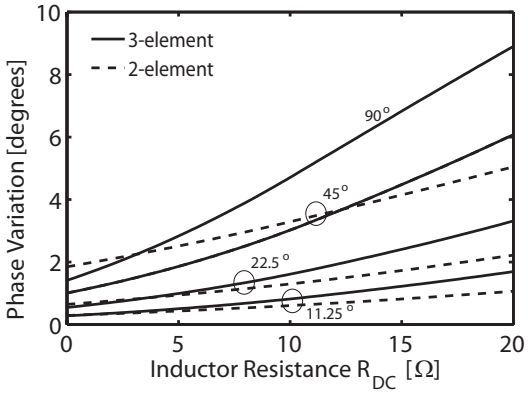

Figure 15: Relative phase variation for three-element bits in $.8w - 1.2w$ band with R_{DC} swept from 0-20 Ω.

3.3.2 Effects from Self-resonance

If the inductor is loss-less, (9) simplifies to

$$j\widetilde{X_{N,C_P\neq 0}} = j\frac{L_0' C_P'}{C_P' - L_0'} \tag{13}$$

The transmission phase for the low-pass path is now

$$\phi_{lp} = tan^{-1}\left[-\frac{B(-\frac{(2C-L)L^3}{(C-L)^2} - L^2 + 1) + \frac{2CL}{C-L}}{2(1-\frac{BCL}{C-L})}\right], \tag{14}$$

where $C = C_P'$ and $L = L_0'$. The transmission phase for the high pass-path becomes

$$\phi_{hp} = tan^{-1}\left[-\frac{2X + \frac{CL}{C-L} - \frac{CLX^2}{C-L}}{2(1-\frac{CLX}{C-L})}\right]. \tag{15}$$

Phase variation is increased as w_{res} decreases. However, the origin is now from the decrease of the center frequency of the phase response. Because of this, loss in the inductor will act against the self-resonance, which decreases the phase variation.

To see this interaction between self-resonance and loss, the phase variation from self-resonance for a few cases of loss is examined. Magnetic (R_{AC}) and resistive (R_{DC}) losses affect the behavior slightly differently, and are represented in Figs. 16a and 16b, respectively. R_{AC} (represented as inductor Q caused by magnetic loss alone) will slightly reduce the phase variation for increasingly poor w_{res}, and R_{DC} has a single frequency at which the phase variation is at a minimum. This point corresponds to the combination of R_{DC} and w_{res} that aligns the center of the phase response with 1 w.

3.4 Loading Effects

Components adjacent to the filter sections (such as the SPDT switch) can also impede their performance. To isolate the impact of these switches and other bits on the performance, the passives in the filtering section will be considered ideal. The switch will be modeled with a generic S-matrix specifying S_{21} and S_{11}, which is then converted to an $ABCD$ matrix.

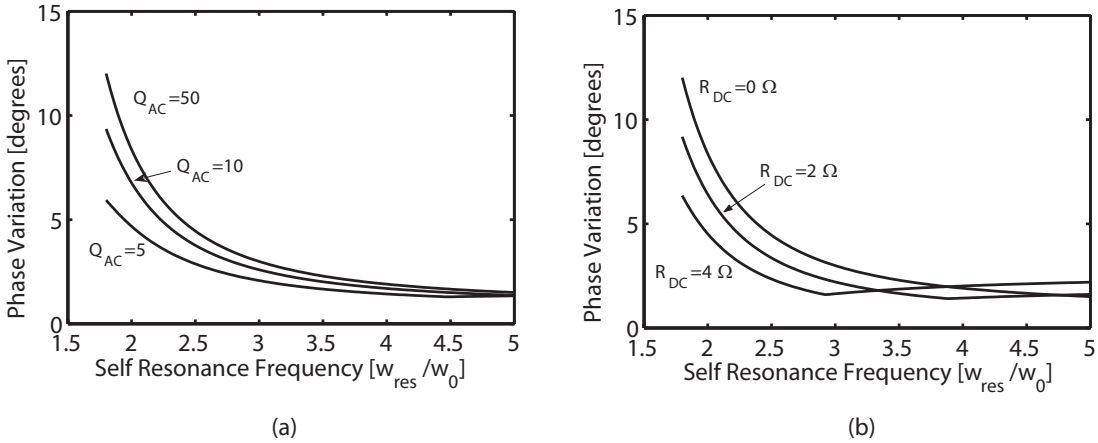

Figure 16: Relative phase error for 90° bit with swept w_{res}: (a) using $Q_{AC} = 50, 10, 5$, where $Q_{AC} = Q$ assuming only magnetic loss contributes ($R_{DC} = 0$), (b) assuming magnetic loss provides $Q_{AC} = 50$, and $R_{DC} = 0, 2, 4\ \Omega$.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{switch} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{bit} \begin{bmatrix} A & B \\ C & D \end{bmatrix}_{switch} \tag{16}$$

The $ABCD$-matrix for this general switch is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{switch} = \\ = \frac{1}{2S_{21}} \begin{bmatrix} (1 - S_{11}^2) + S_{11}S_{21} & (1 + S_{11})^2 - S_{11}S_{21} \\ (1 - S_{11})^2 - S_{11}S_{21} & (1 - S_{11}^2) + S_{11}S_{21} \end{bmatrix} \tag{17}$$

3.4.1 Mismatched Switch With Perfect Isolation

The loss and matching effects of an idealized switch can be modeled using an $ABCD$ matrix given directly by the desired S-parameters. The impact of SPDT match on the frequency and phase shift at the local minimum in the phase response of a bit depends on the type of reactance seen by the filter sections, shown in Fig. 17.

A switch with S_{11} on the real axis will cause the phase response to shift higher in value but remain at the same center frequency. Rotating counter-clockwise, the phase response

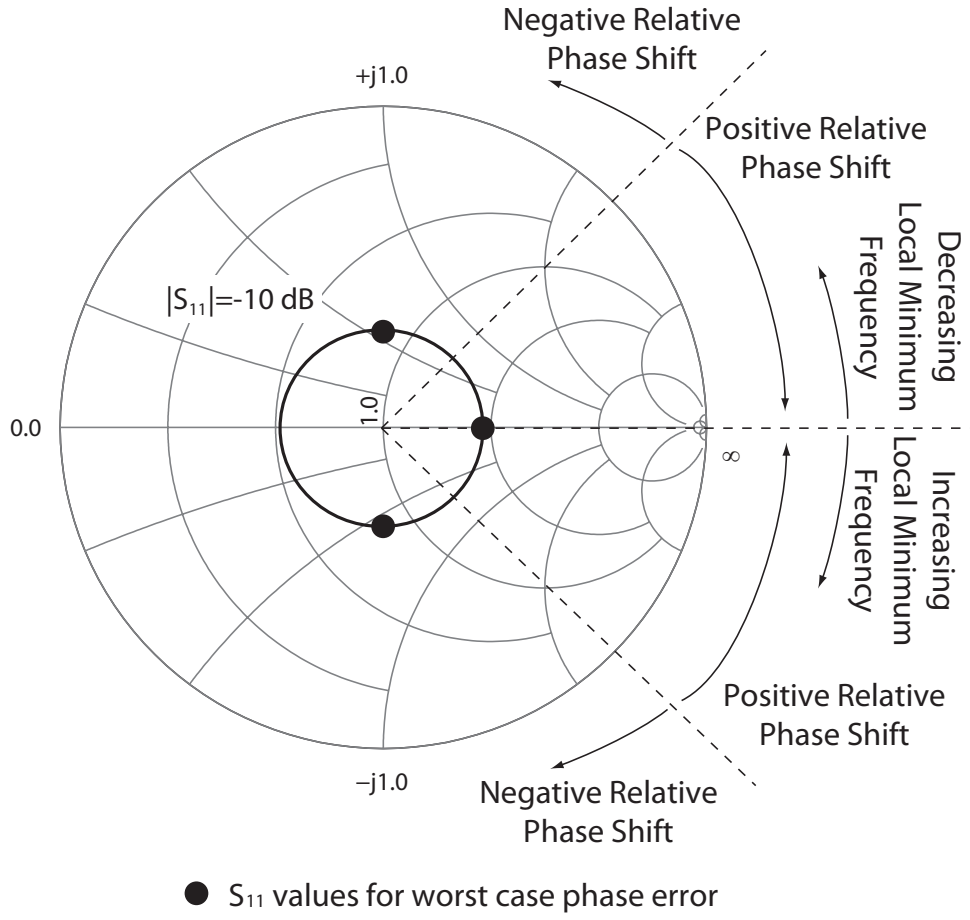

Figure 17: Smith chart showing regional behavior of SPDT match on the frequency of and phase shift at the local minimum in the phase response of a bit. Marked points indicate extremes used as bounds in the analysis.

will decrease in value, eventually dropping below the desired phase shift. In conjunction with this, the frequency of the local minimum will also decrease. When moving clockwise from the real axis, the phase shift at the local minimum will decrease, but the frequency at which it occurs will increase.

The points marked in Fig. 17 indicate the complex values of S_{11} that exhibit the worst phase degradation. S_{11} for a real switch could be anywhere in between these extremes; however these values provide a bound for the phase variation caused by the match of the switch alone. As seen in Fig. 18, all bits have less than 5° phase variation for a SPDT S_{11} better than 10 dB, which quickly deteriorates as the match gets worse.

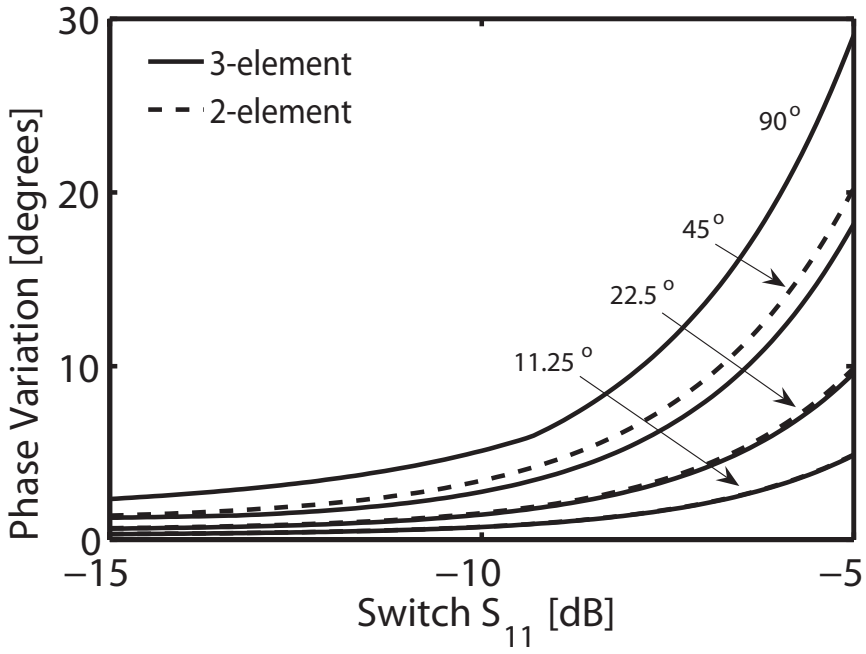

Figure 18: Relative phase error produced by poor switch return loss for single bits.

3.4.2 Effects from Switch Match and Loss for Two Bits

When two bits are used together, each bit is subject to loading from the other bit and the switches, which further complicates overall phase performance. As before, degradation in S_{11} has an impact on the amount of shift at the local minimum and may change the frequency at which the local minimum occurs. Unlike the single bit case, S_{21} now provides a level of load buffering that can improve phase performance at the cost of total phase shifter loss. Figure 19a shows the phase response for the 90° and 45° bit placed adjacently with the same switch model as before in between and on each end with swept S_{11} and S_{21}. An increase in switch loss will result in an improvement of phase error for a given switch return loss. This is due to reflections being attenuated within the switch, which then act as a buffer for problems from loading.

3.4.3 Effects of Finite Isolation

When an SPDT switch with finite isolation is used to select the high- or low-pass paths, some amount of power will flow through the isolated path, resulting in a decrease in the

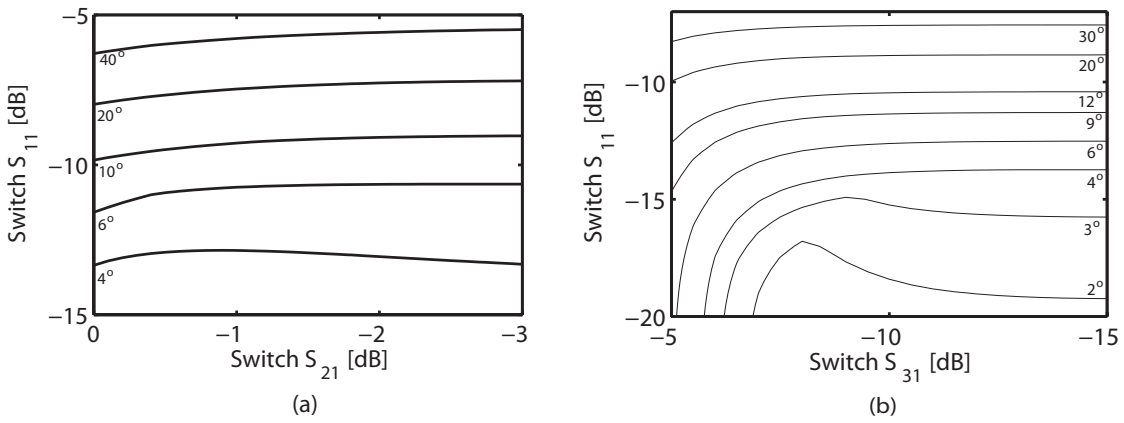

Figure 19: Absolute phase error contours for 90° and 45° bits (a) against switch reflection S_{11} and insertion loss S_{21}, (b) against switch reflection S_{11} and isolation S_{31}.

amount of phase shift. As shown in Fig. 19b, S_{31} has virtually no impact until it is worse than -7 dB. Even in the unlikely event that S_{31} is worse than this, the effect is much less significant than that produced by S_{11}. The impact on phase performance from the isolation between the paths (S_{23}, S_{32}) is essentially non-existent.

3.5 Optimal Bit Ordering

As the previous sections have shown, individual bit performance can be degraded by loading from adjacent bits. To minimize such problems, it is helpful to keep bits with the worst match isolated from each other by placing them in between the best matched bits – particularly if they are more lossy. From Table 4 it appears that larger shift value bits offer the worst match. In reality, however, the opposite is true for two reasons: loss and parasitics. Because the higher shift value bits have larger series inductors in the low-pass path and more elements in each path (which increases routing line losses), they tend to have more loss than the lower shift value bits. This additionally improves their match, as reflections are also attenuated within the bit.

Parasitics introduced from the component layout have a much larger impact on the smaller bits, as the values in the low-pass paths are very small in value and approach that of layout parasitics. Because of these effects, lower shift value bits tend to be the worst matched and most unpredictable, and hence should be separated by the higher shift value

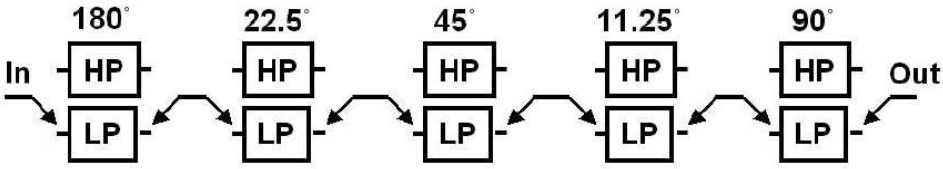

Figure 20: Block diagram showing optimal bit ordering for an optimal five-bit phase shifter.

bits. We have found the optimal bit order to be $180° - 22.5° - 45° - 11.25° - 90°$, as shown in Fig. 20.

3.6 Implementation and Measurements

A fully-monolithic, X-band, five-bit high-low pass phase shifter was designed and fabricated [10] in the commercially available IBM 8HP SiGe HBT BiCMOS technology [28], using the optimization methodologies presented in this work. The phase shift of the analytical model, the simulated design, and the measurement results of the 45° bit is shown in Fig. 21. To provide the best absolute phase variation over X-band, the phase shift was made lower than called for in the analysis (which seeks to make the local minimum 45°). The measured and modeled shifts are in very good agreement, with only a slight change of the local minimum to lower frequency and an increase in shift of less than 0.3 degrees. By designing this bit for slightly less than 45°, an absolute phase error of less than 1° across X-band has been achieved.

The measured insertion loss and return loss of the complete phase shifter can be seen in Figs. 22a and 22b, showing an average insertion loss of -16 dB and a return loss greater than 10 dB across the band of operation for both ports. The circuit also yielded an IP_{1dB} of 4.4 dBm and an IIP3 of 18 dBm, while dissipating 248 mW from a 2.3 V supply.

The absolute and relative phase performance for this shifter over 8.5 – 10.5 GHz is shown in Fig. 29 as RMS phase error for each state. An absolute phase error less than 6° and a relative phase error less than 3° have been achieved. A summary of measurement results is given in Table 5.

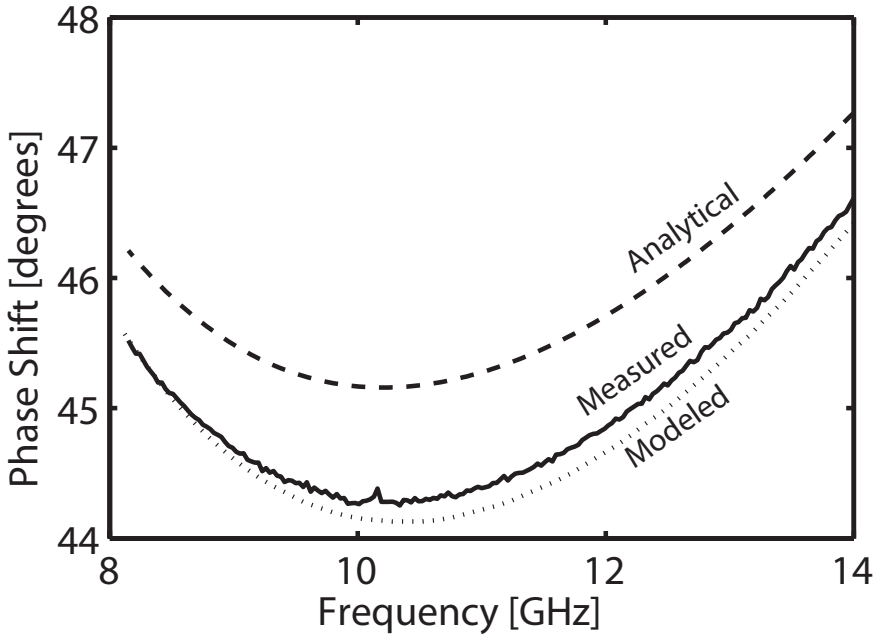

Figure 21: Comparison of the phase shift from the 45° bit produced by the analysis in this paper, a bit modeled carefully prior to fabrication, and a measured device.

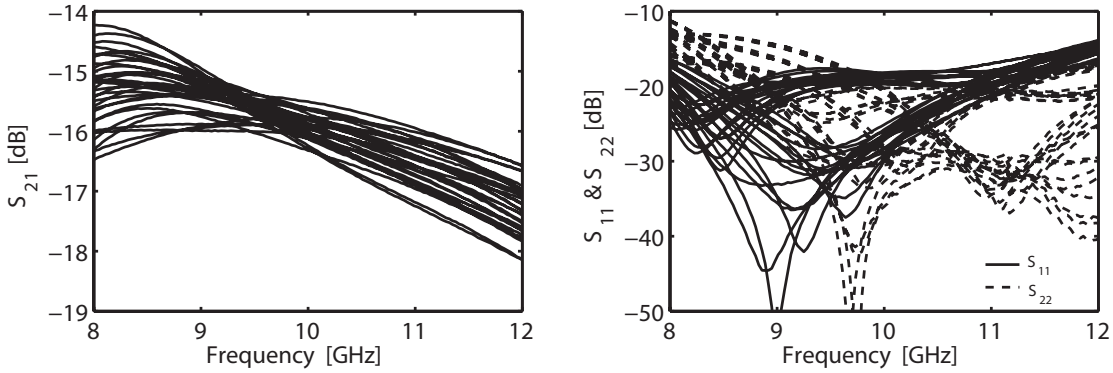

Figure 22: Measurements of five-bit phase shifter. (a) Insertion loss, (b) Return loss.

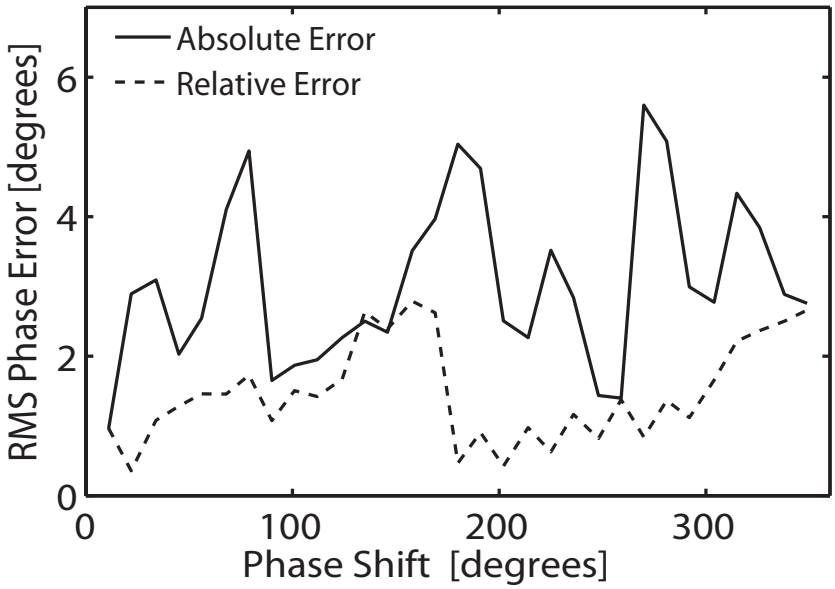

Figure 23: Absolute and relative RMS phase error of five-bit phase shifter in 8.5 – 10.5 GHz bandwidth.

Table 5: Measurement results for five-bit phase shifter

Frequency [GHz]	8-12	8.5-10.5
Insertion Loss [dB]	< 18	< 17
Return Loss [dB]	> 11	> 13
Abs. RMS Phase Err	$< 8^\circ$	$< 6^\circ$
Rel. RMS Phase Err	$< 8^\circ$	$< 3^\circ$
Drive Power [mW]	< 248	< 248
Die Area [mm]	4.1 x 2.4	4.1 x 2.4

3.7 Summary

A comprehensive impact of the major causes of performance degradation in silicon-based, monolithic high-low pass phase shifters with non-ideal components has been examined. Using two elements in filter sections as opposed to three allows for more reasonable device values at the cost of $VSWR$ and bandwidth, particularly for higher shift values. Series resistance and self-resonance in inductors can cause a shift in the location of the local minimum in phase, resulting in poor relative phase variation. The match of switches has a significant impact on bit performance, which can create compounding problems in multiple-bit shifters. Some of these problems are difficult to circumvent because of the fabrication constraints in silicon-based design platforms (e.g., inductor parasitics and transistor performance in the switches); however, intelligent bit ordering helps to mitigate these effects.

For operation at X-band, the high-low pass phase shifter remains a highly competitive topology because of its wide band of operation and reliable and predictable phase shift. The frequencies at this band dictate passive device values well-suited to on-chip fabrication and allow for easy integration into larger systems such as single-chip T/R modules implemented in SiGe technology.

CHAPTER IV

HYBRID PI/T TOPOLOGY FOR REDUCED SIZE PHASE SHIFTERS

With phase performance not dependent on the lossy transmission lines inherent to monolithic technologies in silicon, not only is significant reduction in size possible, but also a reduction in amplitude variation across different phase states. Because the phase shifter dominates the die-area of a monolithic T/R module, its size becomes a cost driver for phased array radar system applications.

This chapter investigates how further reductions in die-area for a monolithic high-pass/low-pass phase shifter can be realized using a hybrid pi/t-network topology for the passive filter sections. A hybrid-topology 5-bit digital X-band phase shifter was designed, fabricated, and tested utilizing a 200 GHz, 0.13 μm SiGe BiCMOS technology [28]. Size and performance characteristics are presented as a contrast to an all-pi phase shifter recently presented by the authors [10] utilizing the same SiGe BiCMOS technology and design goals. With similar bit passive performance to the all-pi design, the hybrid shifter allows for a total shifter die-area reduction of 50.5%.

4.1 Hybrid Bit Topology

The hybrid bit topology consists of a t-network for the high-pass path and a pi-network for the low-pass path. This exchanges one of the inductors for a capacitor, causing both paths to contain a single inductor. A schematic of the bit passives can be found in Fig. 24. The value of the elements in the bits is determined by:

$$B_N = tan(\Delta\phi/4) \tag{18}$$

and

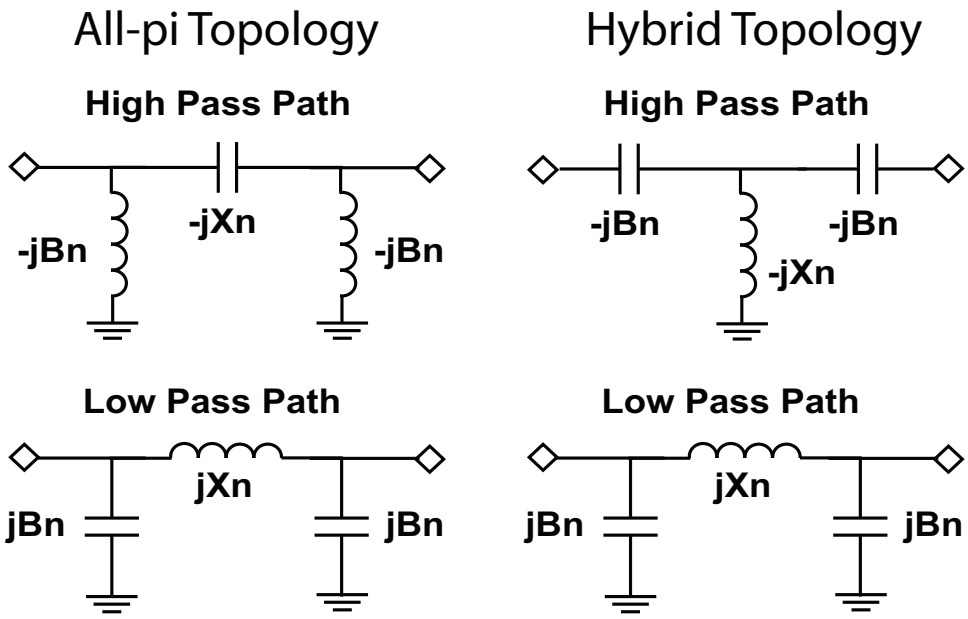

Figure 24: All-pi and hybrid high-pass low-pass filter sections with $B_N = tan(\Delta\phi/4)$ and $X_N = sin(\Delta\phi/2)$.

$$X_N = sin(\Delta\phi/2), \tag{19}$$

where X_N and B_N have been exchanged in the t-network [19].

Skin effects, substrate losses, and other parasitics cause inductors to produce a larger contribution of bit phase error and loss than capacitors in monolithic processes [48]; hence, the hybrid topology used here will generally provide an increase in bit performance. However, the largest advantage to this approach is in both reduction in bit size and the high aspect ratio of the bit.

Inductors are much larger than their related capacitors, but also require sufficient space between them to minimize parasitic coupling. For the all-pi 90° bit in Fig. 25, two inductors are required for the high-pass path resulting in a width of 400 μm. With the hybrid version of the same bit, also shown in Fig. 25, the width is decreased both by the width of the removed inductor and by the spacing that was present between them. This results in much smaller bit die-area, and also changes the aspect ratio of the bit from approximately 1:1 to 1:2.

A high aspect ratio in the bit reduces the die-area of phase shifters in a straight-line

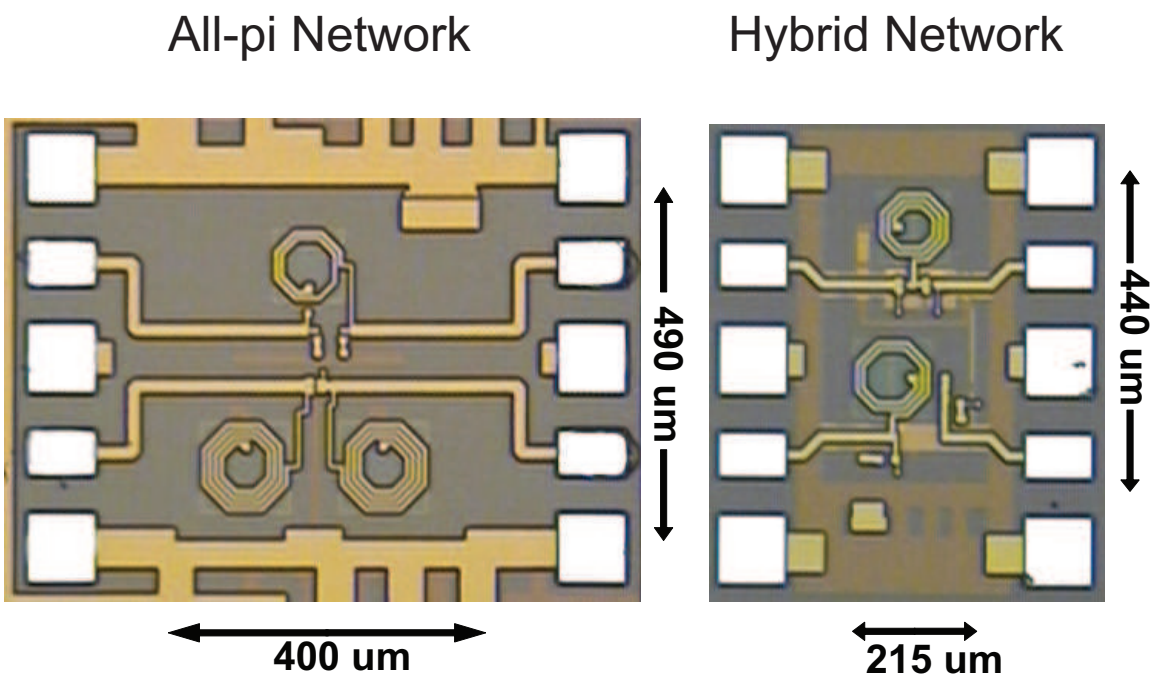

Figure 25: Die photo of all-pi 90^o in [10] and the present hybrid 90^o bit.

layout by reducing the length by the same amount the bit-width has decreased. Greater die-area reductions can be realized in a meandered S-shaped layout. With SPDT switches forming a right-angle, very narrow bits will minimize the dead-space that occurs between the upper, middle, and lower paths of the phase shifter. This translates into further die size reductions for the full shifter, while still maintaining a reasonable aspect ratio. This can be seen in the die photos of the all-pi and hybrid phase shifters in Fig. 26, with the hybrid shifter occupying approximately half of the area as the all-pi shifter.

4.2 Implementation and Measurements

A fully-monolithic, X-band, 5-bit, high-low pass phase shifter was designed and fabricated [10] in the commercially-available IBM 8HP SiGe HBT BiCMOS technology [28], using the hybrid network topology to minimize die area. The measured insertion loss and return loss of the complete phase shifter can be seen in Figs. 27 and 28, showing an average insertion loss of -20 dB, and a return loss greater than 13 dB across the band of operation for both ports. The bit elements account for $2.5 \pm 0.2\ dB$ loss with the total switch loss contributing between $15.5 - 22.5\ dB$.

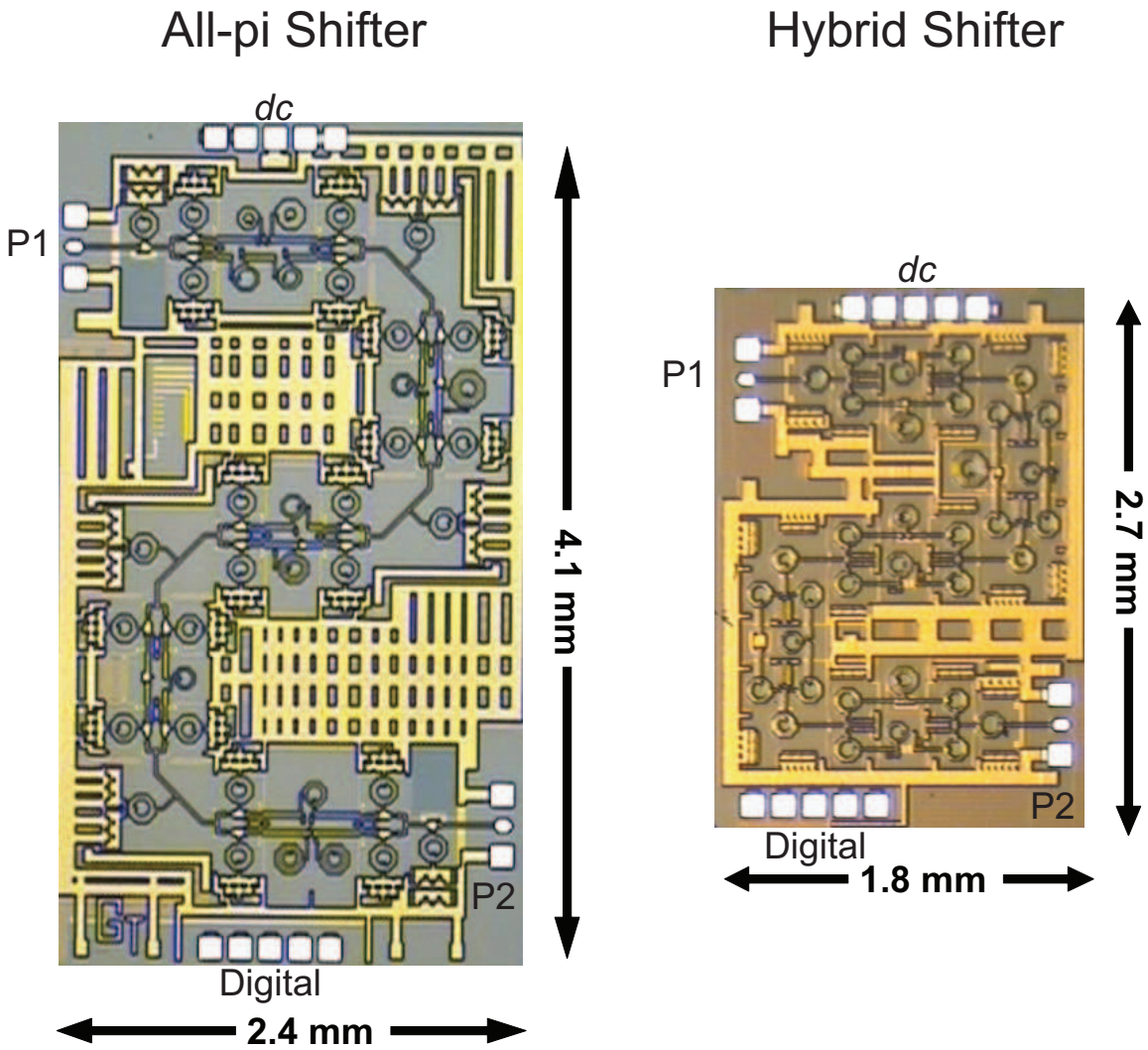

Figure 26: Die photo of all-pi phase shifter in [10] and the present hybrid phase shifter.

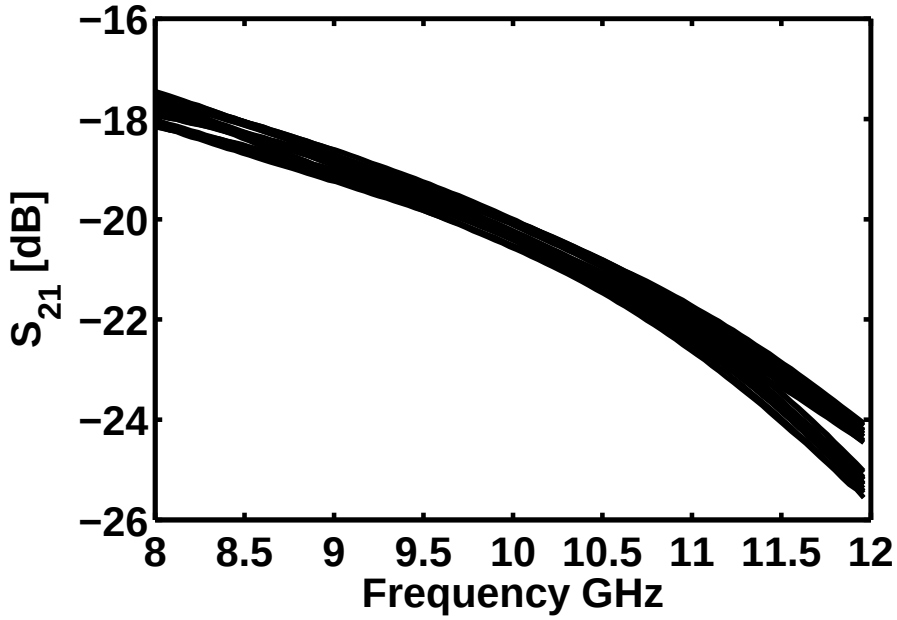

Figure 27: Measured insertion loss of 5-bit hybrid phase shifter.

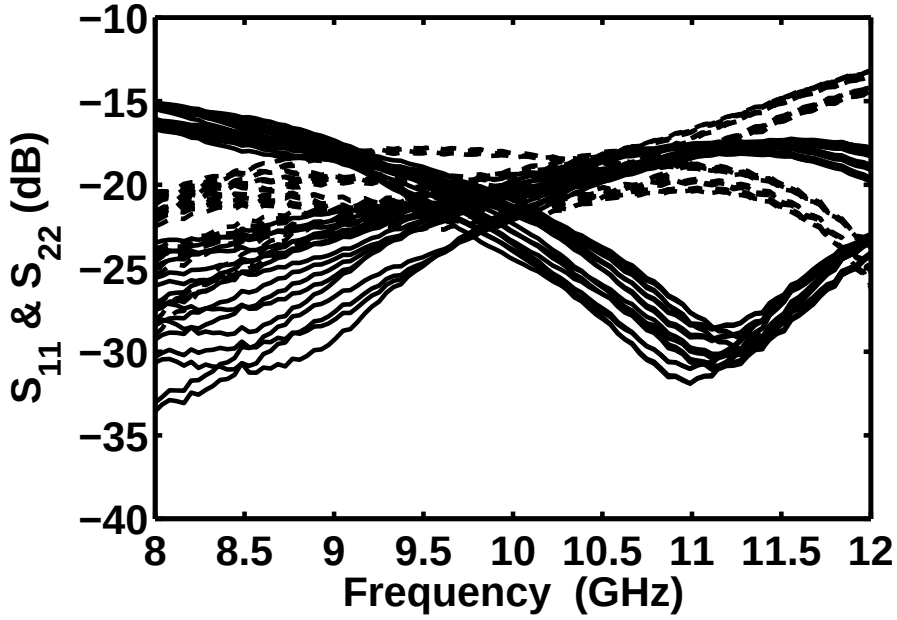

Figure 28: Measured return loss of 5-bit hybrid phase shifter.

The phase shift of the present hybrid phase shifter can be seen in Fig. 29. The circuit achieves a constant and predictable phase shift over the frequency of operation, and an absolute phase error (Fig. 30) of less than ± 13° across 8 GHz to 12 GHz.

4.3 Discussion

An error in the design of the 180° bit led to a shift in the phase performance when the bit is in the active (on) state, producing the notably different family of curves shown in Fig. 30. When this bit is inactive, absolute phase error remains lower than 5°. However, total hybrid shifter phase performance remains comparable to the all-pi shifter, and acceptable for the intended application.

A summary of measurement results and a comparison with the all-pi network in [10] is given in Table 6. The higher total shifter loss of the hybrid approach is attributed to higher loss of the MOS switches used, in comparison to the HBT switches employed in the all-pi shifter. Loss attributed to the bits, however, is slightly lower in the hybrid approach. One fewer inductor per bit allows for an overall average decrease of 0.5 dB. The use of MOS switches also accounts for the large (favorable) reduction in power consumption, and is hence represents a fundamental tadeoff. Most notably, however, the die area required for the hybrid shifter is approximately half that of the all-pi shifter, clearly a dramatic improvement. Because the hybrid bit passives can be made very narrow, dead space in an *S*-shaped phase shifter can also be minimized.

4.4 Summary

A hybrid pi/t bit passive topology that reduces the die-area of the high-pass/low-pass phase shifter has been presented. A 5-bit X-band phase shifter with digital control was designed with this technique in 130 nm SiGe BiCMOS technollogy, with measured performance comparable to the much larger all-pi design. The circuit can provide 360° of phase shift, and an absolute phase error less than ± 13° over the entire band of operation. The shifter achieves an average insertion loss of -20 dB, and maintains a return loss greater than 10 dB for all states over the band of operation. Total shifter die-area was 4.87 mm^2, more

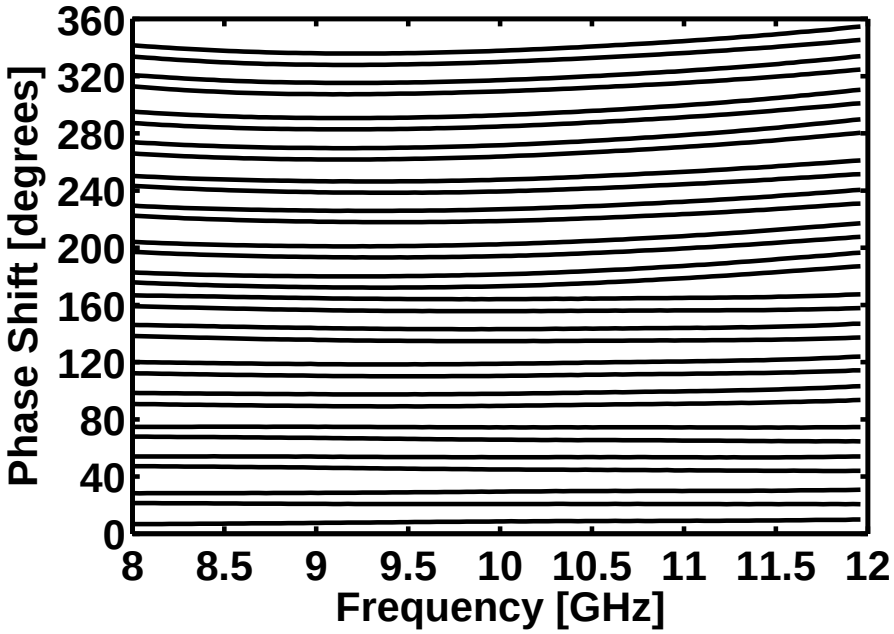

Figure 29: Phase shift for hybrid-topology 5-bit X-band SiGe CMOS phase shifter.

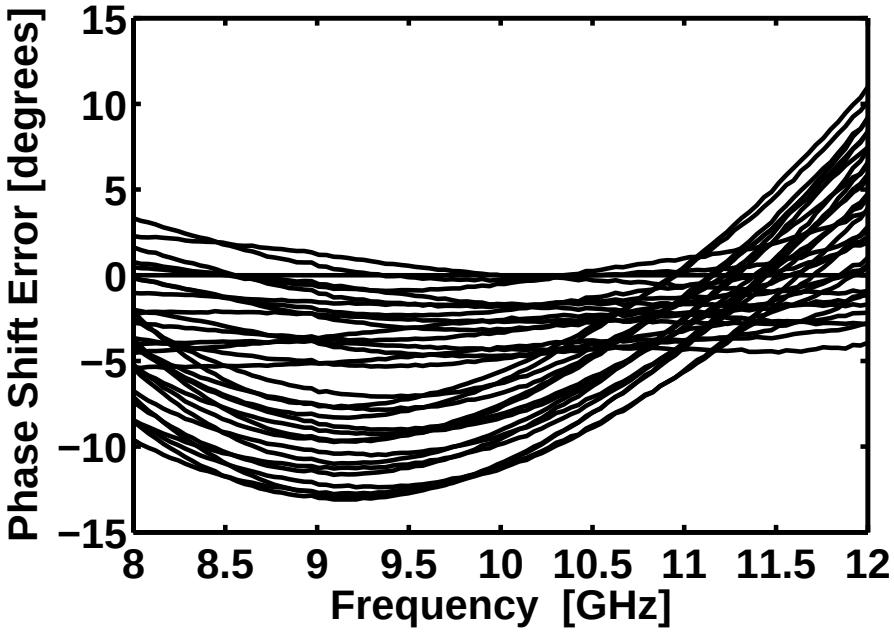

Figure 30: Absolute phase error for hybrid-topology 5-bit X-band SiGe CMOS phase shifter.

Table 6: Performance comparison of all-pi and hybrid topology four-bit phase shifters

	All-pi Topology [10]		**Hybrid Topology**	
Frequency [GHz]	8.0-12.0	8.5-10.5	8.0-12.0	8.5-10.5
IL [dB]	< 18	< 17	< 25	< 21
Return Loss [dB]	> 11	> 13	> 13	> 15
Phase Error [deg.]	< 15	< 8	< 13	< 13
Power Dis. [mW]	248		< 1	
Die Area [mm^2]	9.84		4.87	
Passive IL [dB]	< 3.2		< 2.7	
Passive RL [dB]	> 14		> 14.5	
Passive Phase Error [deg.]	< 8		< 9	
Passive Area [mm^2]	0.6965		0.4466	

than 50% less than the all-pi shifter area of 9.84 mm^2. Achieving equivalent performance in half the size of the all-pi topology, the cost-saving potential of the hybrid pi/t topology for high-pass/low-pass phase shifters in monolithic radar systems has been demonstrated.

CHAPTER V

SPINEL MAGNETIC NANOPARTICLE THIN FILMS FOR REDUCED-SIZE INDUCTORS AND DELAY LINES

A reduction in the die-area required for a phase shifter would be of great benefit if loss and phase performance could be maintained. Although new topologies for transmission line based phase shifters have been proposed [34], their size is still heavily dependent on the wavelength of the band of operation. Similarly, the size of the High-pass/Low-pass phase shifter is attributed in large part to the size of the inductors. A technology to reduce the size of both of these elements with minimal performance degradation would provide great benefit for both the phase shifters and the systems they support.

Thin films with relative permeability greater than one allow for much larger effective phase constants than nonmagnetic materials. This effect reduces the physical size of microwave circuits, and provides interesting applications in a diverse area of microwave design such as phase shifters and inductors. Results have been reported for ferroelectric thin films in the past. However, the large relative permeability of the presented magnetic thin film has many advantages over the ferroelectric materials. The electrical properties of $CoFe_2O_4$ spinel magnetic nanoparticle films are currently unknown, but these materials may provide a significant effect on the effective phase constant. This chapter presents the fabrication process of such thin films, as well as measured data and simulations of transmission lines using this new film technology.

5.1 Spinel Magnetic Nanoparticle Thin Films

$CoFe_20_4$ spinel magnetic nanoparticle samples are prepared via normal micelle microemulsion methods [59]. Nanoparticles with size $\sim 1Onm$ were chemically bound to silicon substrates using silane self-assembly methods and particle surface derivatization techniques. To create an amine-coated substrate, silicon wafers were soaked in a solution of

3-aminotriethoxysilane (1 % v/v in $EtOH$). The amine-modified substrate was dipped into a solution of $CoFe_2O_4$, nanoparticles whose surface had been coupled with an imidazole carbonate. Nucleophilic substitution by the surface amine occurs. The wafer is then immersed into a second solution of the $CoFe_2O_4$ nanoparticles whose surface had been modified with aminobenzoic acid. The amine surface on the nanoparticle will couple to the particles bound on the silicon substrate through nucleophilic substitution with the free imidazole on the particle surface that was not involved in coordination to the glass slide. By alternating from a solution of amine-coated nanoparticles to an imidazole-coated particle solution, films of known thickness are created by adding successive particle layers. A $CoFe_2O_4$ sample with film thickness of 100 nm was fabricated on 400 μm thick high resistivity silicon ($\rho > 10k\Omega cm$).

Finite Ground Coplanar (FGC) structures were fabricated as shown in Fig 34. Two layouts were chosen based on the amount of phase shift produced from Momentum simulations, one with a signal width (s) of 50 μm, ground widths (B) of 250 μm, and slot widths (w) of 33 μm, and one with s = 50 μm, B = 250 μm, and w = 60 μm, Values used for the Momentum simulation assumed relative permittivity of 1 and a relative permeability of 100 for the film.

Using the AZ 5214 photoresist and the lift-off process, a metal thickness of 6500 Angstroms was achieved and no detrimental effects to the film were observed. The metal for the film sample and comparison sample was deposited simultaneously to minimize variance in conductor thickness between the two. TRL calibration standards were fabricated on both samples.

5.2 Measurements

The effective combined dielectric/magnetic constant ($\varepsilon_{eff}\mu_{eff}$), incorporating both the effective permittivity and effective permeability, and loss were extracted from a NIST (National Institute of Standards and Technology) TRL calibration on both the magnetic film sample, and the high resistivity silicon sample for comparison. The measured effective combined constant, shown in Fig 34, indicates that the 100 nm film increases the constant by

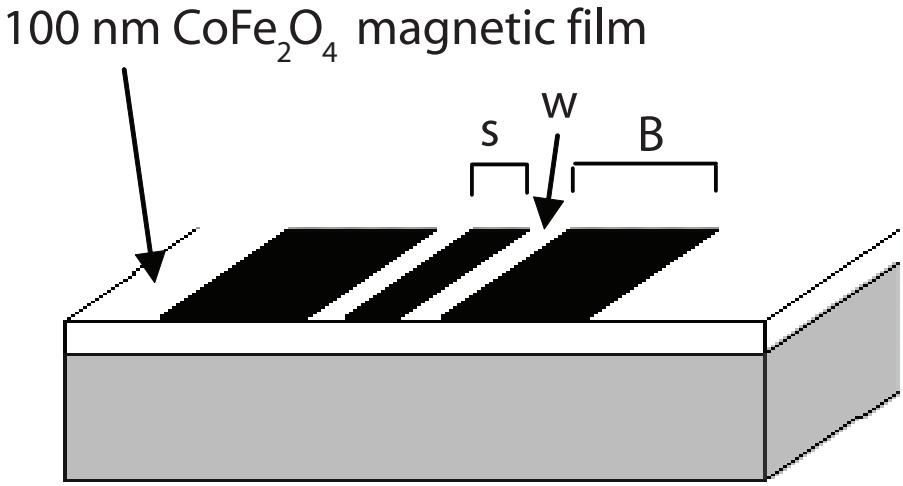

Figure 31: Schematic diagram of FGC line with nanoparticle thin film.

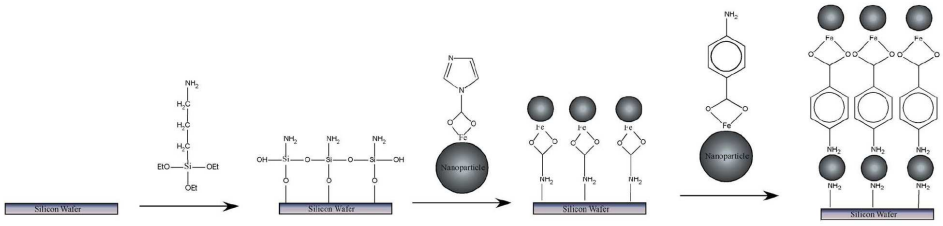

Figure 32: Schematic of $CoFe_2O_4$, spinel magnetic film coating process.

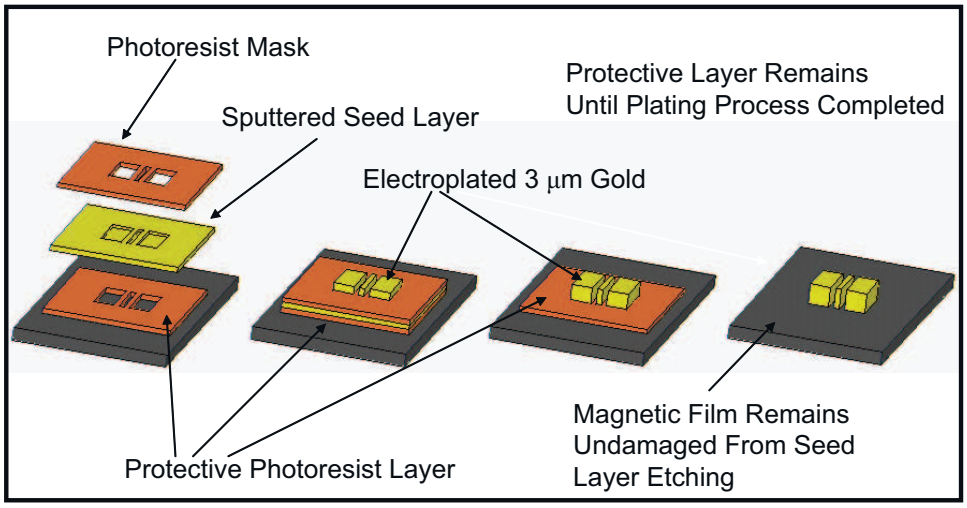

Figure 33: Protective electroplating fabrication process. The fragile nanoparticle film is shielded from the hydroflouric acid solution with a photoresist barrier.

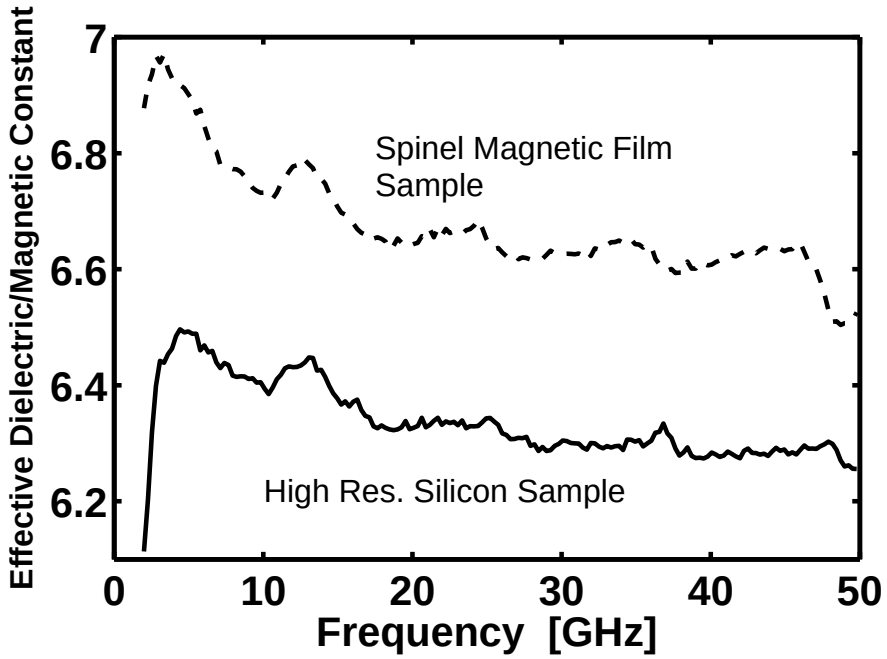

Figure 34: Measured Effective Dielectric/Magnctic Constant. Extracted from NIST TRL calibration, this shows the increase in the effective combined constant over a broad range of frequencies.

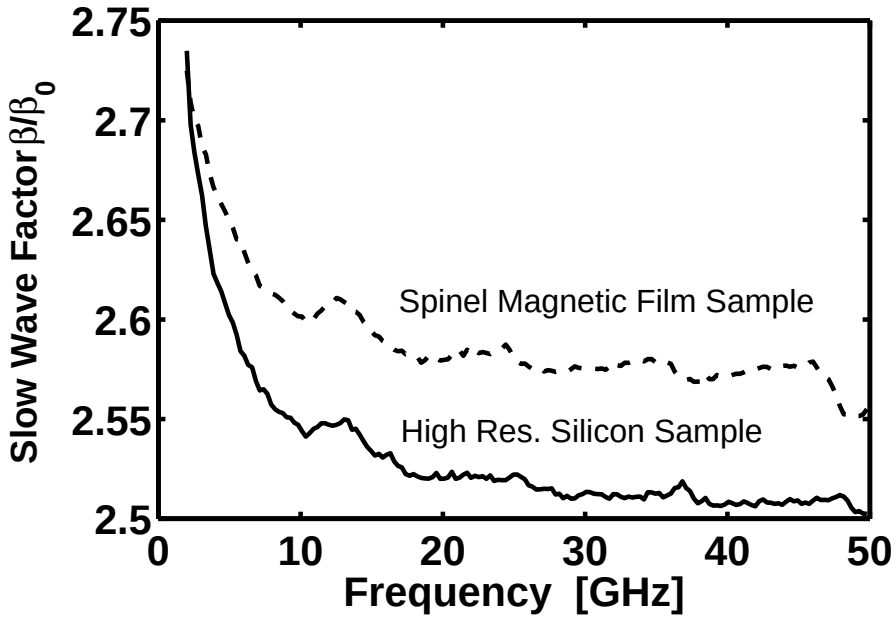

Figure 35: Measured Slow Wave Factor. Extracted from NIST TRL calibration, this shows the increase in the slow wave factor.

approximately 0.3 (4.7% increase). The slow wave factor, shown in Fig 35, indicated the 100 nm film increases the slow wave factor by approximately 0.07 (2.8% increase).

The loss is shown in Fig 36. Because of the thin metallization layer, skin depth effects greatly increased the measured loss. The characteristic impedance is also changed by the film due to the increase in inductance, as

$$Z_0 = sqrtL/C \tag{20}$$

The relative permittivity and relative permeability can not be isolated in the effective combined constant alone, so capacitors were fabricated to determine the relative Permittivity independently. The $CoFe_20_4$ film was grown on a Silicon sample with a thick metal layer, and multiple small circular aluminum patches were sputtered using a shadow mask.

Capacitance measurements were taken with an Agilent LCR meter, and the relative permittivity was extracted using:

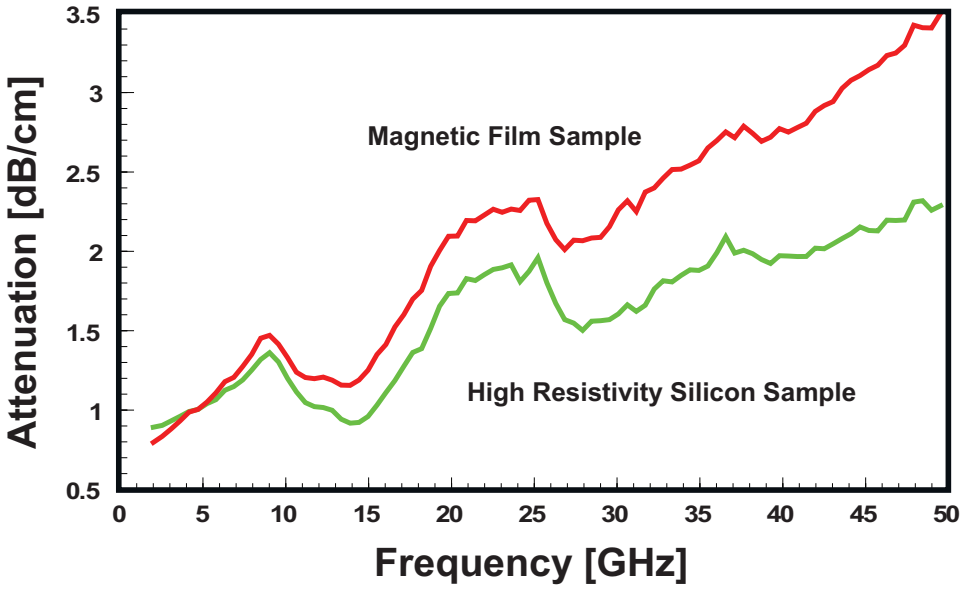

Figure 36: Measured Attenuation. Extracted from NIST TRL calibration. this shows the attenuation of the CPW lines. However, skin depth and variance in the characteristic impedance degrade the accuracy of this comparison.

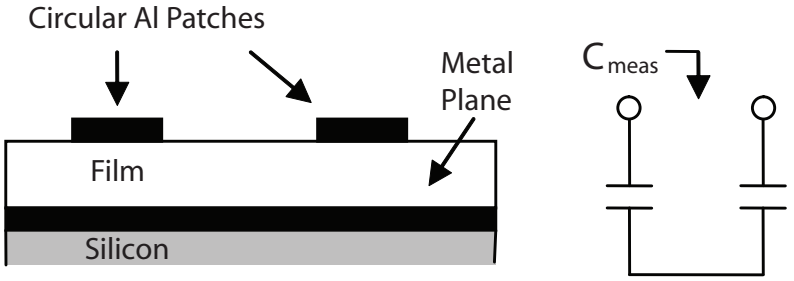

Figure 37: Cross-sectional view of capacitors and equivalent circuit.

$$\varepsilon_r = 2C_{meas}t/\varepsilon_0 A \tag{21}$$

where C_{meas} is the measured capacitance between two patches, t is the thickness of the $CoFe_20_4$ film, and A is the area of the patch. Numerous measurements were taken and averaged to take non-uniformity of the film into account. The relative permittivity of the film was determined to be approximately 1.

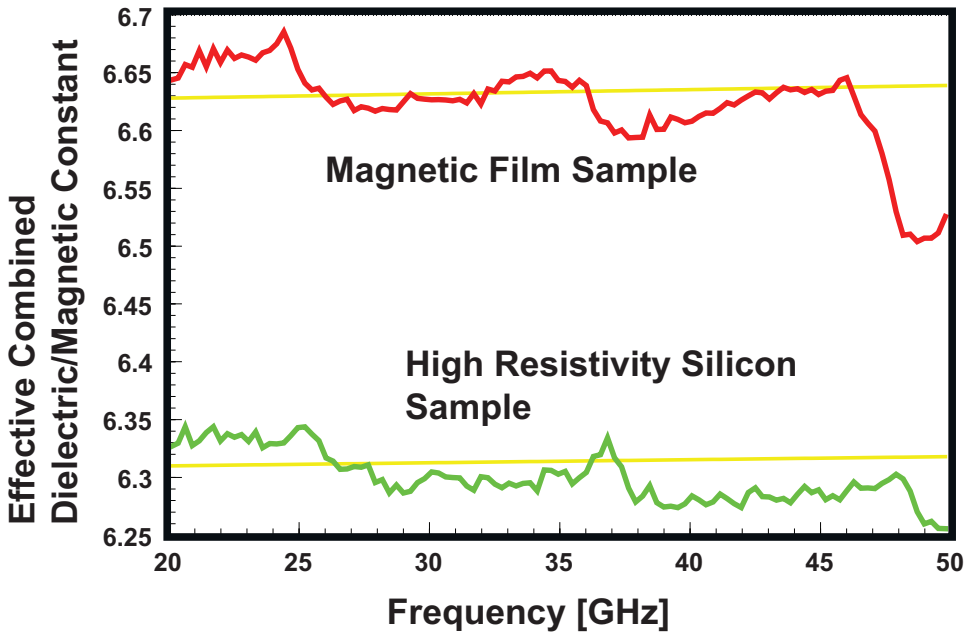

Figure 38: Simulated and Measured Effective Dielectric/Magnetic Constant. SONNET simulations of possible relative permeabilities for the magnetic film and relative permittivities for the high resistivity silicon samples along with the measured data.

5.3 Simulations

The CPW structures were modeled in SONNET to determine possible values of the relative permeability for the magnetic material assuming a relative permittivity of 1 ($\varepsilon_r = l$). The results are shown in Fig 38. The effective dielectric constant was best matched using a relative permittivity of 11.6 for the high resistivity silicon sample, that produced an effective dielectric constant of approximately 6.3. The effective combined dielectric/magnetic constant for the magnetic film is approximately 6.63 (5.2% increase) over the frequency range of 20 - 50 GHz, and a value of 59 for the relative permeability for the magnetic film best matched the measured data. The simulated effective dielectric/magnetic constants appear as nearly straight lines in the figure. The simulated characteristic impedance is increased from 51 Ω to 58 Ω using $\varepsilon_r = 1$ and $\mu_r = 59$.

With the relative permittivity and permeability of films determined, it is now possible to accurately model the film for use in specific applications. A relative permeability of 59 provides a significant increase in the effective phase constant for a very thin film, and shows much potential for applications such as phase shifters and inductors.

CHAPTER VI

RF MEMS PACKAGING METHODS

RF MEMS switches may provide substantial advantages in the insertion loss and isolation of switches in circuits such as a phase shifter, but they are not without significant drawbacks. Of primary concern with this chapter is that of the need for hermetic packaging.

The electrostatic force required to actuate a MEMS device is very small (on the order of 100 μN), as is the opposing force caused by the spring section of the membrane itself [6,16,36,64]. Due to the very low actuation voltage used for the designed switch topology ($\sim$ 22 V), stiction can become a problem. If impurities, particularly water vapor, are present in the ambient atmosphere surrounding the MEMS device, the slight surface tension present at the membrane-dielectric interface can create a force that exceeds that of the opposing spring force. In this situation, the MEMS membrane remains in the down-state, irrespective of applied actuation voltage. The MEMS device in this essentially permanent state renders the circuit or system it supports dysfunctional. In addition, water molecules are a vehicle for contaminants like negative (Cl , F, NO_3, SO_4, PO_4) and positive (Na, K) ions that cause performance degradation [41].

As such, the advantages offered by the MEMS switch technology cannot be achieved without an appropriate package that will both protect the device from hostile environments and allow for low-loss RF and DC signal transition in and out of the package [15, 20, 49, 73].

Two packaging methods will be discussed in this chapter. The first is a traditional thermal compression bonding technique, with a new and high-performance interconnect technology compatible with commercial IC fabrication. The second method investigates the first localized heating technique for packaging RF MEMS with LCP.

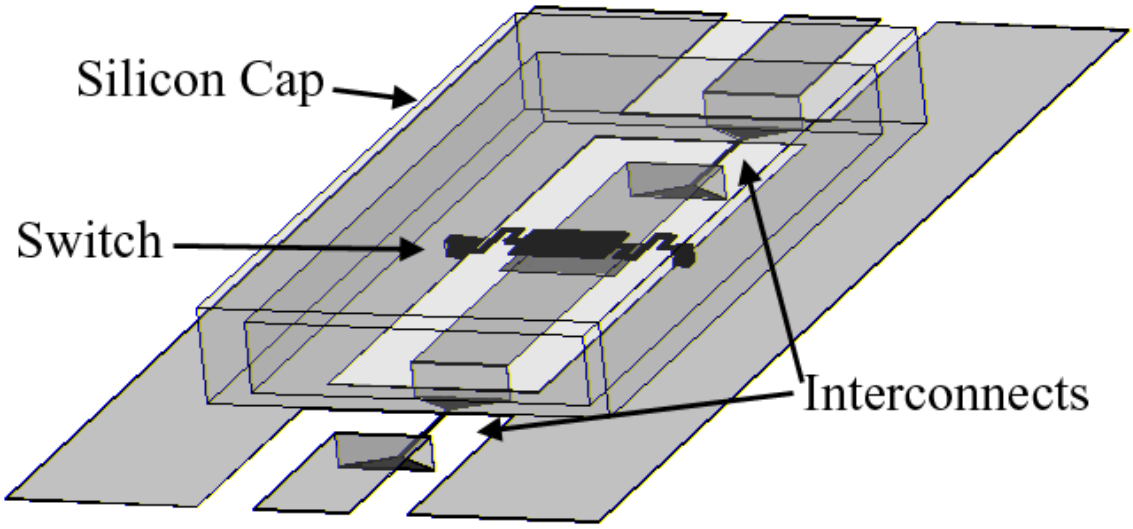

Figure 39: Conceptual drawing of a capacitive membrane switched packaged with a thermal compression bonding method.

6.1 Thermal Compression Bonding on Silicon

For packaging RF MEMS switches, an interconnect is required that is able to pass both RF and DC signals with minimal loss and large bandwidth (Fig. 39). Because lines must be kept small and vias through the substrate would be required for a microstrip line, FGC lines are more practical. For compatibility with IC fabrication techniques, only a thin oxide layer will be used. This allows for system-on-a-chip (SOC) integration. For thermal compression bonding, a gold ring enclosing the MEMS device must reside on top of the oxide layer, and signal lines passing in and out of the package must pass under the bonding ring between the silicon and the oxide layer (Fig. 40).

6.1.1 Interconnect Design

The restriction of a thin oxide layer complicates the design, as the electrical effects of the bonding surfaces play an essential role in RF performance. This is especially true for packaging with thermal compression bonding, as a gold ring must fully enclose the perimeter of the device to be packaged. However, thermal compression bonding has advantages over methods such as anodic bonding (which does not require a metal ring), because package RF shielding is simple to achieve, the bonding surfaces can be fabricated simultaneously

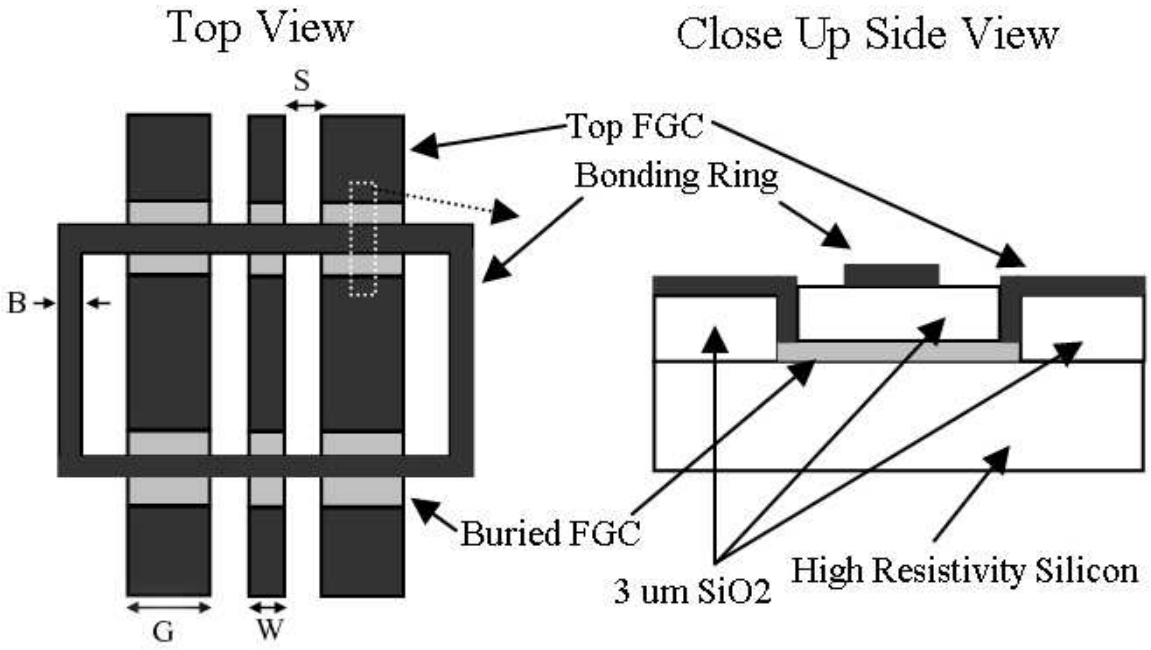

Figure 40: Top view of simple FGC interconnects with bonding ring (width B varies from 20 μm to 200 μm depending on design) and side view close up of signal line in interconnect region. The CPW line is located underneath the oxide layer, attaching with upper CPW line outside and inside the bonding ring with vias. The CPW signal width W is 150 μm, with ground widths G of 300 μm and gap spacing S of 90 μm.

with the MEMS device and the overall cost is low. With an unbroken gold bonding ring surrounding the packaging region, an interconnect must pass through on a separate layer. However, if a finite ground coplanar (FGC) line simply passes underneath the bonding ring while buried under a layer of SiO_2 (Fig. 40), two significant problems occur. The first and most noticeable effect is the attenuation that occurs at the interconnect. This happens because the ground and signal lines are capacitively coupled to the bonding ring, effectively producing a microstrip mode of very low characteristic impedance. This results in an impedance mismatch and causes high reflection. For example, with an oxide thickness of 3 μm, ground widths of 300 μm, signal line width of 150 μm with 90 μm spacing and a bonding ring width of 200 μm, a capacitance of about 1 pF and 0.5 pF can be expected between the bonding ring and the ground and signal lines, respectively (by parallel plate approximation). While this may not pose a problem at low frequencies, the impact of this capacitive coupling can become very detrimental as the frequency of operation increases.

The second problematic effect arises in the implementation of such an interconnect with

a system such as a switch. If, for instance, a switch packaged with this interconnect were performing a perfect short internal to the package, RF energy would capacitively couple to the bonding ring, and resonate to the opposing line. To overcome these problems, we first consider an interconnect as a buried FGC line as before, but with the ground lines connected electrically to the bonding ring. This can be accomplished either by etching the oxide and fabricating vias directly between the bonding ring and FGC ground lines, or by simply allowing the ground lines to continue on the top surface of the oxide to meet with the bonding ring and keeping the signal line buried as before. This resolves the isolation problem, but now greatly increases the microstrip moding effects seen in the previous example. As the ground lines are now electrically connected to the bonding ring passing above the buried signal line, we essentially have a short section of microstrip at the interconnect region. Two challenges exist with this: a sudden change from coplanar field patterns to microstrip field patterns cannot happen, and the characteristic impedance of the microstrip line in the interconnect region has an extremely low impedance of only a few ohms since the metal width is large compared to the thickness of the oxide separating it from the now grounded bonding ring. These two problems can be overcome simultaneously by providing a coplanar-to-microstrip transition region in the immediate vicinity of the bonding ring (Fig. 41)

6.1.2 Simulations

To find the proper geometries for the buried interconnects, Ansoft HFSS was used. An oxide thickness of 3 μm was chosen because of its compatibility with standard IC fabrication. The geometries of the ground and signal lines were determined, leaving only the length of the transition region as a variable. The transition is similar in nature to the CPW to microstrip transition presented in [79], except that the bonding ring that serves as the microstrip ground is directly connected to the FGC ground lines, and the signal line is routed through a via underneath the oxide layer. The width of the buried line decreases linearly from the FGC signal width to the microstrip width between the via and the bonding ring, allowing for a smooth transition from CPW modes to microstrip modes. The opposite transition

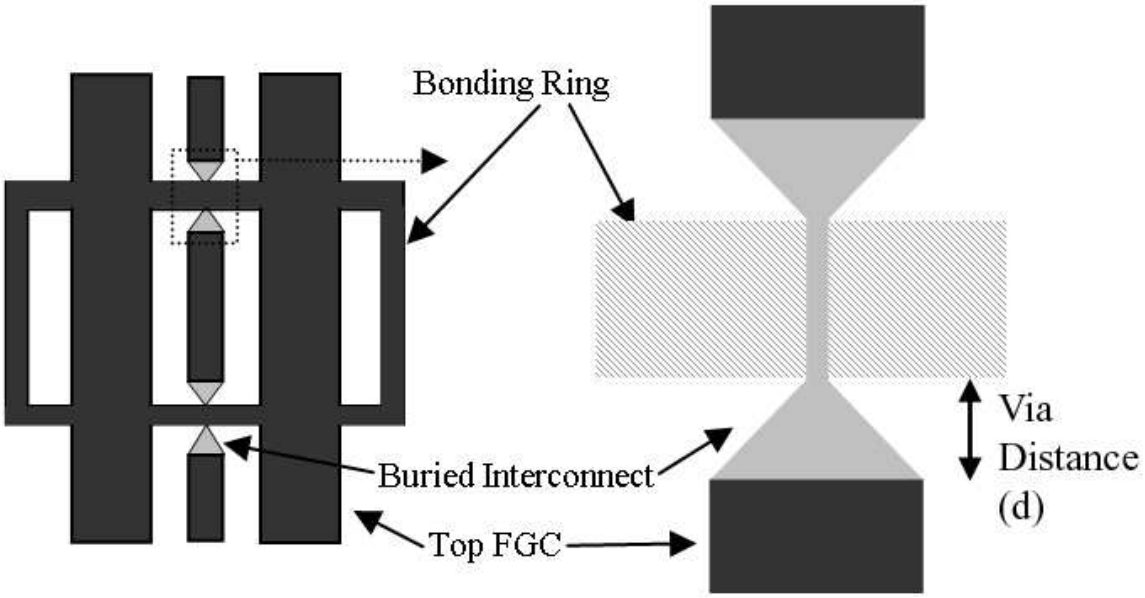

Figure 41: Top view of modified interconnections with bonding ring and top view close up of buried layer. The bonding ring is on same layer and directly connected to the FGC lines on the top layer. The bonding ring is shown patterned in close up view to allow modified interconnect to be seen

takes place on the other side internally to the bonding ring, allowing the FGC line to once again be on top of the oxide layer. Parametric sweeps were run to determine the optimum distance (d) of the via from the bonding ring. This optimum distance was found to be 50 μm. Simulation results for distances of 40, 50, and 60 μm are shown in Fig. 42 and show the sensitivity to this variable. The characteristic impedance of the microstrip region is 42 Ω (to reduce resistive losses with a wider line at a slight impedance matching expense) and 52 Ω for the FGC line.

6.1.3 Fabrication

The structure shown in Fig. 41 was fabricated on high-resistivity silicon ($\rho > 28$ kΩ/cm). The buried interconnects were first metallized by depositing 300 Angstroms of Ti with 6000 Angstroms of Au, and then etched to obtain numerous test structures with a variety of microstrip widths. A thin metal thickness for the buried line was required to achieve a sufficient level of planarity of the top of the oxide layer for bonding. A 3 μm thick layer of silicon dioxide was deposited by PECVD, and the vias were etched by RIE. The FGC lines,

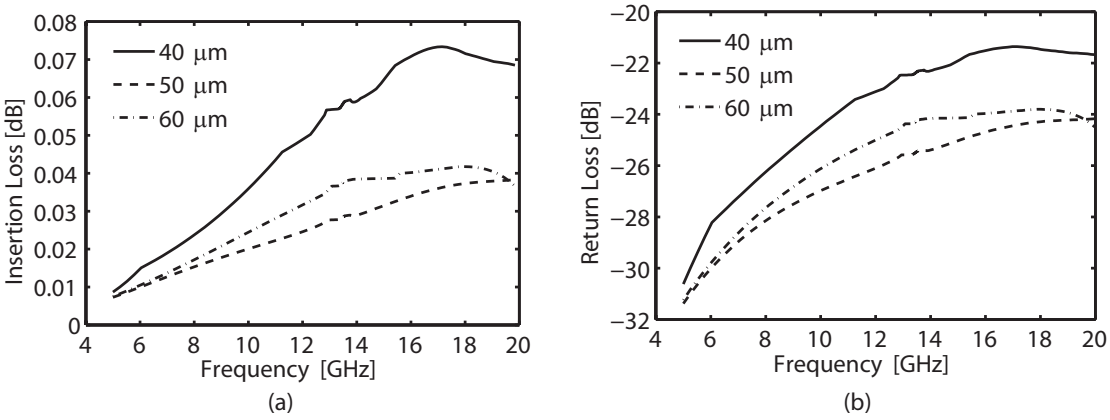

Figure 42: Sensitivity of via distance (d) in simulations. Reflection (S11) and Insertion Loss (S21) of a single interconnect from Fig. 41 (right side) with via to bonding ring distances of 40, 50 and 60 μm.

bonding ring, and vias were metallized simultaneously by sputtering on a seed layer of 200 Angstroms Ti, 2000 Angstroms Au, and 200 Angstroms Ti. The lines were then built up by electroplating to a thickness of 3 μm, resulting in the structure shown in Fig. 43.

The cap wafer is fabricated by bulk micro-machining a silicon wafer. Both SiO_2 and SPR-220 photoresist are used as masking layers to create cavities and windows for measurement in a single etching step with deep-RIE. This creates 150 μm deep cavities with well-defined rings that bond to the bonding rings on the MEMS wafer, and windows etched completely through the wafer to allow for measurement. A 2 μm layer of Au is then sputtered on the cap wafer. Alignment is performed with a Karl-Suss BA6 wafer aligner. Bonding is achieved at 200° C with a tool pressure of 2000 mBar under vacuum.

Figure 44 shows an SEM of a cavity on the cap wafer after a bonded sample has been pried apart. Au has been torn off on the right and left sides, and significant roughness can be seen on the etched portion of the sample. This roughness is a product of the etching process, but since it is 150 μm above the MEMS wafer it has no negative impact on performance.

6.1.4 Measurements

Measurements were performed from 2 - 50 GHz using an HP 8510 Network Analyzer with a NIST TRL [43] calibration, bringing the measurement reference planes to 200 μm away

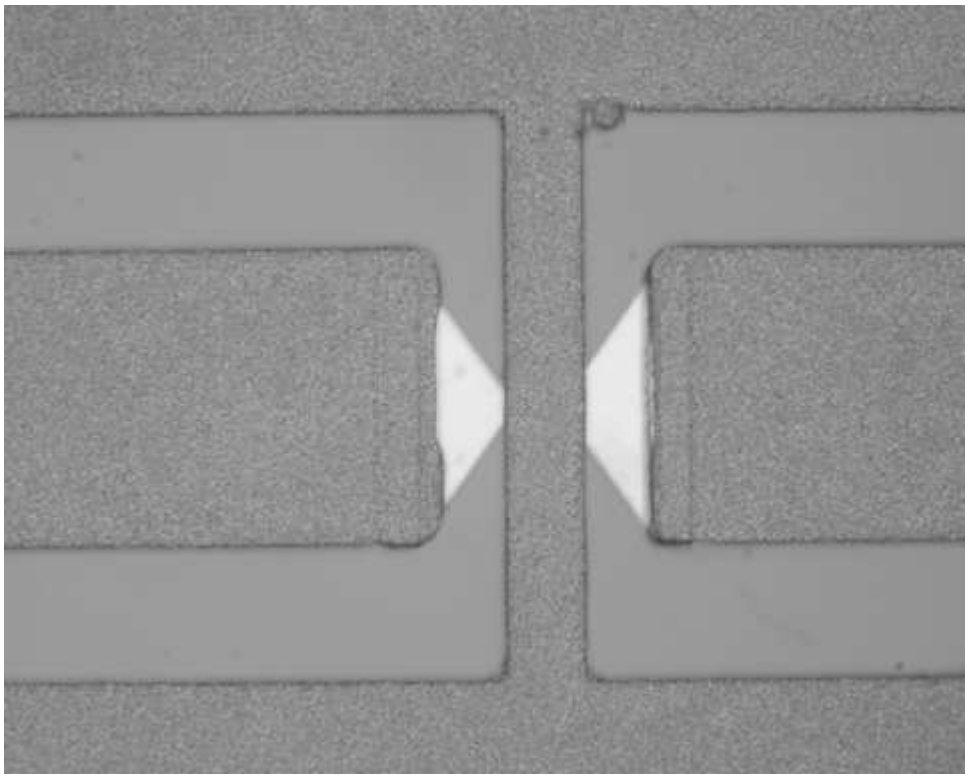

Figure 43: Close up of transition. The 8 μm wide microstrip line lies underneath the 50 μm wide bonding ring but its profile can be seen from the bump in the oxide and the bonding ring metallization. The distance between the vias and bonding ring is 50 μm.

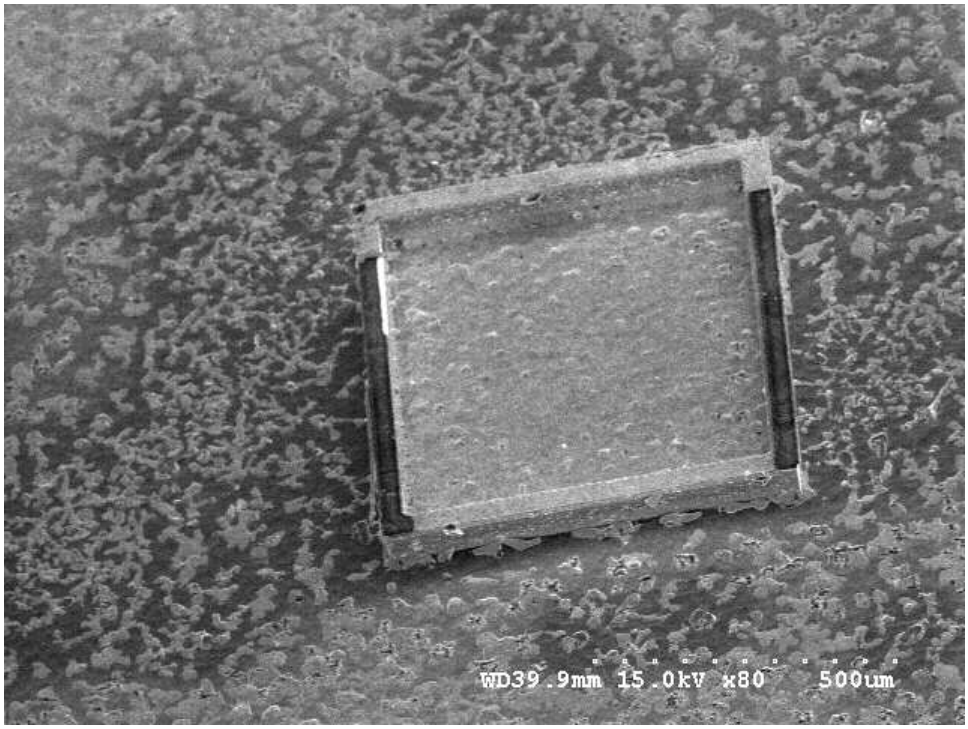

Figure 44: SEM of cap wafer with cavity after forcibly removed from bonded sample. Au has been removed from the left and right sides during separation.

from the external vias. The insertion loss of back-to-back modified and simple interconnects is shown in Fig. 45a. The reflection from these structures is shown in Fig. 45b.

The measured attenuation from the modified interconnect is largely independent of frequency, and shows a loss of approximately 0.25 dB for a single interconnect. The loss of the modified structure can be greatly attributed to the small microstrip width, which was optimally 8 μm for a 3 μm thick oxide layer. A thicker oxide may be used to reduce the resistive losses, as wider microstrip lines would be implemented. Doing this would also allow for a thicker metallization for the buried line, as the planarity of the oxide layer above the transition would be less sensitive.

Measurements of the MEMS switch with interconnects were performed from 20 - 90 GHz, bringing the reference planes to 200 μm away from the bonding ring. The insertion loss for the switch in the up-state and isolation in the down-state is shown in Fig 46a. At the resonant frequency of 57 GHz, the loss is 0.3 dB for the up-state with a difference between states of 33 dB. Loss in the up-state stays below 0.5 dB up to 65 GHz, and below

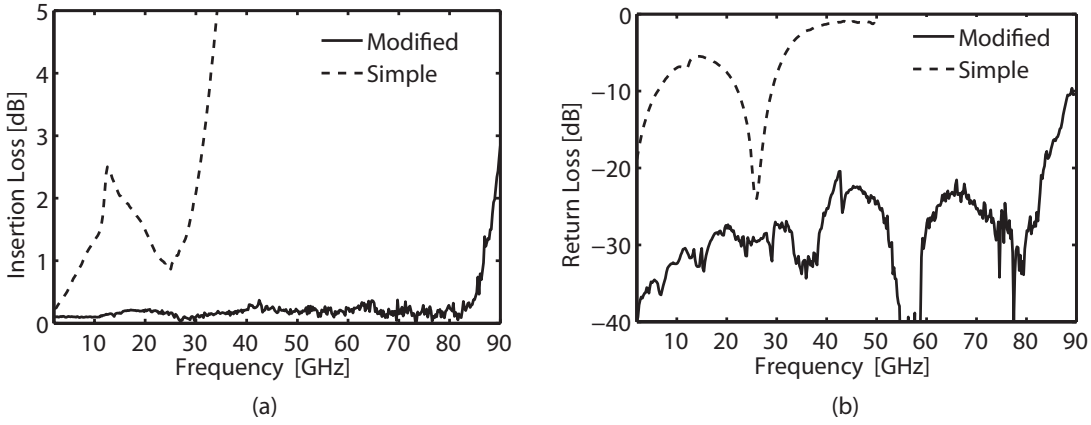

Figure 45: (a) Measured insertion loss of back-to-back interconnects. (b) Measured reflection of back-to-back interconnects. Large reflection for simple case shows that capacitive coupling on wide signal line causes impedance mismatch.

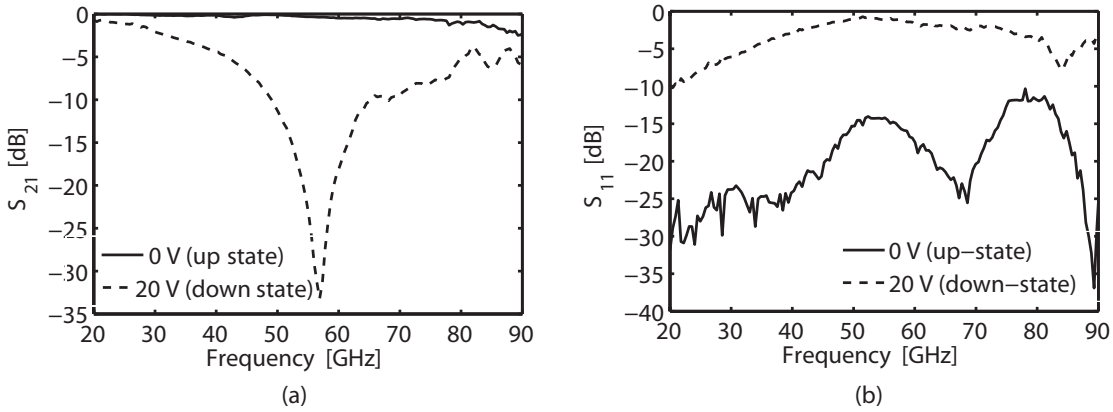

Figure 46: Measurements of MEMS Switch. (a) insertion loss / isolation, (b) reflection.

1 dB up to 83 GHz. Isolation is better than 10 dB from 50 to 65 GHz. The reflection for both states can be found in Fig 46b.

6.1.5 Packaging

The switch sample fabricated for packaging suffered from minor fabrication problems in the final membrane etching step. Because of issues with the resist used to define the aluminum membrane, the membrane was was not flat after it was released, leading to increased loss and degraded reflection. This also led to difficulties in switch activation and bad down-state performance. The degradation in performance can be seen in the difference between

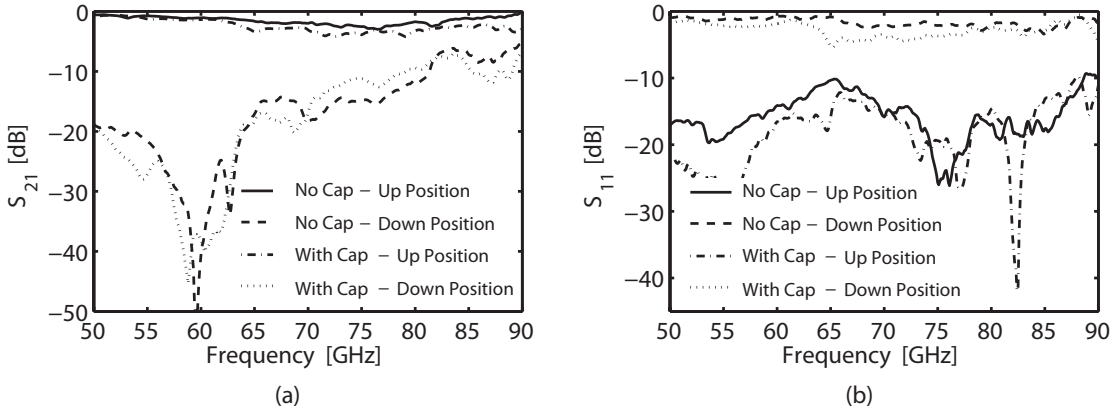

Figure 47: (a) Measured insertion loss (up-state) and isolation (down-state) of switch with and without un-bonded manually-aligned cap wafer. (b) Measured Reflection for up and down states for switch with and without un-bonded manually-aligned cap wafer.

measurements of the switch in Fig. 46a and the measurements of the switch sample for packaging in Fig. 47a.

However, when the cap wafer was placed on top of the sample, manually aligned and weighted down, no significant change in S_{11} was seen. This is evidence that the bonding cap has little effect on the performance of the switch, which is expected since the RF path is shielded from the cap by the upside-down microstrip region at the interconnect interface.

Measured insertion loss and isolation can be seen in Fig. 47a for the switch-package sample with and without an un-bonded cap. The isolation is very similar between the two, and differences in loss may be from mechanical stress on the membrane caused by the manual alignment of the cap. The difference between S_{21} for the up-state in the packaged and un-packaged cases is negligible. Performing the alignment with a wafer aligner will remove this problem since the alignment is performed while the wafers are out of contact. The reflection for the up and down states for the switch-package sample with and without un-bonded caps can be seen in Fig. 47b. Again there is some discrepancy between the packaged and un-packaged S_{11} for the down state (isolation), possibly caused by mechanical stress. S_{11} in the up-state, however, is slightly improved in the packaged case. This is due to improving radiation losses.

Table 7: Comparison of the packaging state of the art to the technique presented in this work

	Method Error	Loss (dB)	Band (GHz)	Temperature	Bulk/Surface
Michigan	Thermal Compression	0.08	2-40	300 °C	Bulk
Michigan	Al/SiO_2	N/R*	N/R	700 °C**	Surface
Michigan	Thermal Compression	0.1	15-25	350 °C	Bulk
Alcatel	BCB	0.3	1-10	250 °C	Surface
This Work	Thermal Compression	0.25	0-80	200 °C	Surface

* Not reported. ** Local heating. [2, 42, 68, 76].

6.1.6 Summary

A novel interconnect for use with thermal compression bonding for packages has been demonstrated, with a loss of approximately 0.25 dB per interconnect up to 80 GHz. The flat frequency response of the attenuation provides versatility for packaging applications in any frequency band and is not bandwidth limited. The simple fabrication process allows for the incorporation of package fabrication into the fabrication of internal devices, such as RF MEMS switches or any other such device that may be controlled by DC voltages on the FGC ground and signal lines, and additional DC biasing lines may be fabricated simultaneously. The ability to use thermal compression bonding also allows for a nearly hermetic package with minimal cost and a wide variety of materials that can be used for the cap. Since the bonding ring itself is connected to RF ground, the cap of the package could be trenched in silicon or glass, completely coated with gold. This would allow not only a nearly hermetic seal but RF shielding as well. Because the process is compatible with standard IC fabrication techniques, low-cost integration of this interconnect with an SOC or SOP antenna system is possible. A comparison of this technique to the state of the art is shown in Table 7.

A fabricated RF MEMS switch for 50-80 GHz has also been demonstrated. The switch currently has a resonant frequency of 57 GHz with 0.3 dB loss and 33 dB isolation, which can be further improved with simple modifications in membrane and SiN layer height.

While the measured performance of the switch for packaging was degraded from fabrication problems, the minimal impact of the cap wafer on S_{11} can clearly be seen.

6.2 Localized Packaging with Liquid Crystal Polymer

Liquid crystal polymer (LCP) has recently been shown to be an ideal material both as a substrate for high-frequency RF performance and as a packaging medium because of its very low dielectric loss, near-hermetic nature, and extremely low cost [67]. LCP has also been successfully implemented in the packaging of MEMS sensors [14], and RF MEMS switches [7,8]. However, current packaging methods rely either on low-temperature LCP or intermetallic bonding, that require temperatures in excess of 290°C and 260°C respectively. While these temperatures may be acceptable for certain sensor applications, this temperature exceeds the maximum allowable temperature of popular RF MEMS switch architectures such as the capacitive membrane [56]. Above 200°C, the membrane of these switches suffers from plastic deformation, that have permanent negative effects on the performance of the device. As such, the excellent hermeticity results from the lamination technique described in [8] require temperatures that damage the MEMS devices and degrade performance, seen as poor insertion loss and isolation in the post-bonded switch [7]. Clearly, lamination techniques are not viable for high-performance packaging of temperature sensitive devices.

Localized heating techniques have been used to package temperature-sensitive MEMS sensors using patterned aluminium lines within a stack-up of plastic layers [65], and similar methods have been demonstrated with silicon substrates [76]. This allows for high heat at the bonding regions while the device remains at a safe, much lower temperature. However, embedded metal lines would cause significant degradation in RF performance for MEMS devices.

This chapter investigates the use of patterned lines on copper clad LCP as a low-cost method for packaging RF MEMS switches (Fig. 48). A significant advantage of this method is the use of heating lines external to the stack-up allowing for easy removal and hence no impact on RF performance as seen in previous work. Simulations of the heating element structures are performed to examine the thermal characteristics of the bonded regions and switch. Heating lines are fabricated on LCP requiring only one photolithography and etch step, and the MEMS cavity is formed with two 1 mil layers of low-temperature LCP that are etched with a CO_2 laser system. This laser etch is performed only to quickly etch the

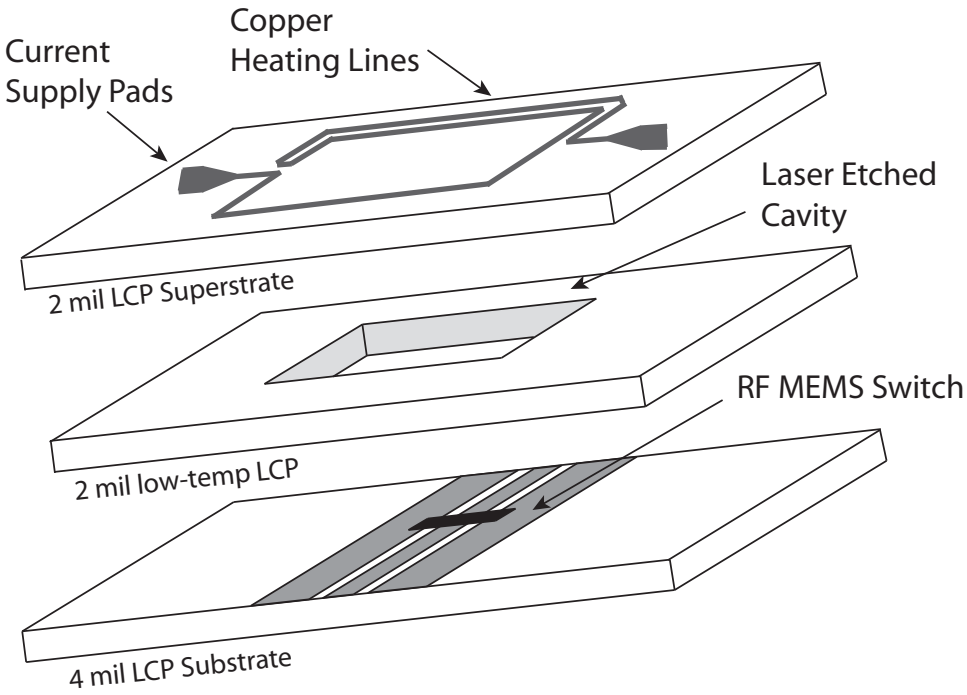

Figure 48: Layer stack-up for localized heating method.

low-temperature LCP layer into cavities for prototyping, not used in forming the seal as in some more complicated bonding methods. The layers are bonded with localized-heating by passing 7 A of *DC* current through the heating element while compressing the 4 layers together. The bonded switch is submerged in 60°C water for 24 hours to test seal quality. Before and after measurements are shown, providing evidence of a successful bond. No lasers or exotic heating materials are required in the sealing process, resulting in a very low cost packaging solution. A low cost localized heating method for temperature sensitive MEMS devices on LCP using the provided copper cladding is shown for the first time.

6.2.1 Implementation

A capacitive membrane MEMS switch is fabricated on 4 mil LCP using a previously published fabrication process [72].

The heating element is fabricated on copper clad 2 mil LCP. 500 μm wide lines are patterned via photolithography and etched in copper etchant. The lines form a rectangular region that encircle the desired bonding area, consisting of 3-4 heating lines per side to facilitate a wider bonding region. The heating lines are tapered out to a large 1 inch wide

line at either end. The large lines provide higher conductivity that generates significantly less heat than the 500 μm lines during bonding and allows easy access for the bonder current supply. Tapers limit excessive heating at the junctions between line widths resulting from high local resistance.

A cavity for the MEMS switch is fabricated from two pieces of 1 mil low-temperature LCP. These layers are etched with a CO_2 laser system to provide room for the switch and contact the area of the heating rectangle on the heating element sample.

The four layers are sandwiched together and pressed between high-temperature glass slides with enough pressure to keep the heating elements from delaminating during heating. Glass was used as it is a poor thermal conductor, which keeps heat generated at the heat elements from sinking to the slides and reducing heat flow to the internal LCP layers. 7 A of *DC* current is applied to the heating element, pulsed at 60 Hz for 30 seconds. Switching the current allows for better thermal transfer vertically through the layers without causing the top layer to heat excessively. Higher currents can be used for faster bond times, but this causes the heat on the top layer to potentially damage the top LCP or copper lines.

The patterned heating elements reside on the topside of the heating layer, so they can be easily etched after bonding. This requires thermal transfer through the top layer, but removes impact of the copper heating lines on RF performance.

The bonding method can easily be scaled up to accommodate multiple individually packaged devices (wafer-scale packaging). Wider lines can be used between bonding regions to limit the areas where the melting temperature is reached. Expanding the bonding area or bonding additional regions simultaneously requires the same amount of current (assuming a constant heating line width is kept at the bonding regions), but higher voltage resulting from the larger resistance seen at the current supply terminals. Using thinner metal layers will result in higher resistance for the same line geometry, trading current requirements for higher voltages. Because the heating lines are patterned, complicated seal shapes and extremely varied seal sizes and geometries can be created for simultaneous bonding at wafer-scale.

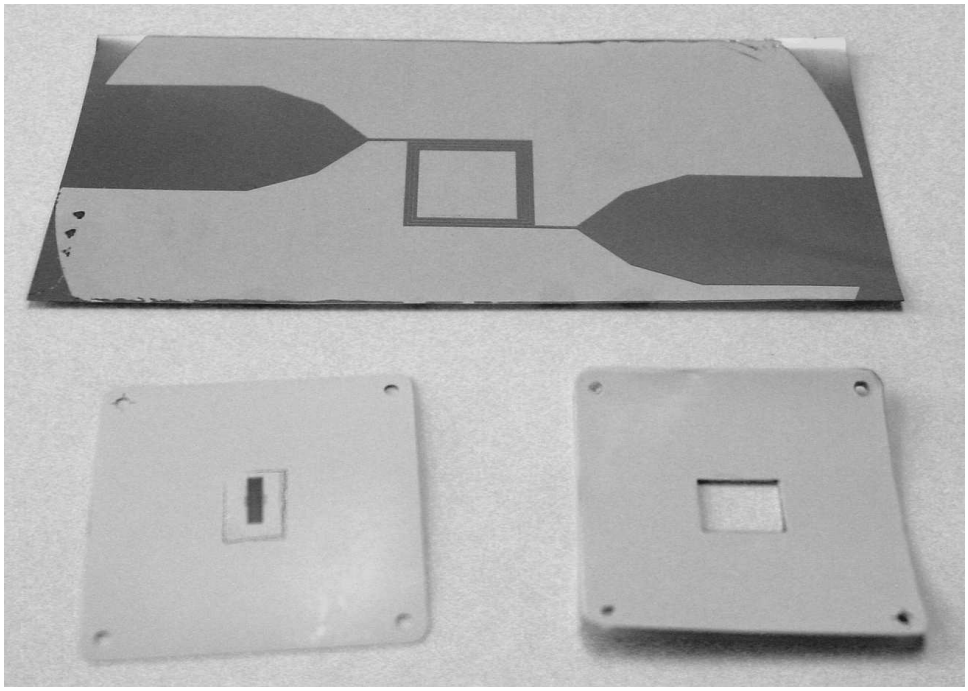

Figure 49: Photograph of heating element superstrate, laser etched spacer layers and MEMS LCP substrate prior to bonding.

6.2.2 Thermal Simulations

FEMLAB 3.1 multiphysics simulator by COMSOL [12] was used to simulate the ring bonding environment. The steady-state, conduction, heat transfer module was used to simulate the transfer of heat to the MEMS switch. Two-dimensional simulations were performed from the top and side perspectives. The impact of the bonding process on the MEMS switch was investigated.

LCP, like most polymers, is a poor thermal conductor. It is about 17 times more conductive than air while silicon is almost 300 times more conductive than LCP. This means it would take significantly more energy to heat up a sample of LCP than it would for a sample of silicon. Since we need to bond layers of LCP using heat, it is important to study how efficiently heat can spread through LCP.

Since a mechanical model is being used, the appropriate physical constants must be entered for LCP. These values are shown in Table 8.

For the first simulation, the entire ring is simulated with enough room around the borders to show the lateral spread of heat. A perfect thermal insulating boundary condition is used

Table 8: LCP material properties [13]

Property	Symbol	Value
Young's Modulus	E	16 GPa
Poisson's Ratio	ν	0.3
Density	ρ	1400 $\frac{kg}{m^3}$
Thermal Conductivity	k	0.5 $\frac{W}{mK}$
Relative Permittivity	ϵ_r	3.1

at the extremities to provide a reference point at room temperature (22°C). The copper lines are heated to 300°C and the package is allowed to reach the steady-state. The results from this simulation are shown in Figure 50.

As desired, the heat spreads very well around the copper traces but do not extend much laterally. This is desired since it is important that the high temperature does not reach the switch.

For the second simulation, a cross section of one side of the ring is simulated with enough depth to show the vertical spread of heat. Again, a perfect thermal insulating boundary condition is used at the extremities to provide a reference point. The copper lines are heated to 300°C and the package is allowed to reach the steady-state. The results from this simulation are shown in Figure 51.

This simulation further demonstrates how poorly the heat spreads laterally. Since LCP will not melt below 290°C, for copper lines heated to 300°C, there is approximately 200μm of vertical bonding. For thicker bonding layers, a higher metal temperature will be required.

From these simulations, it can be concluded that metal ring bonding techniques can be used to package RF MEMS devices.

6.2.3 Measurement Results

The switch was measured from 2-40 GHz on an Agilent 8510C network analyzer with an SOLT calibration. Measurements of the switch were taken before any bonding operations took place. After bonding, the switch was submerged in 60°C water for 24 hours. After

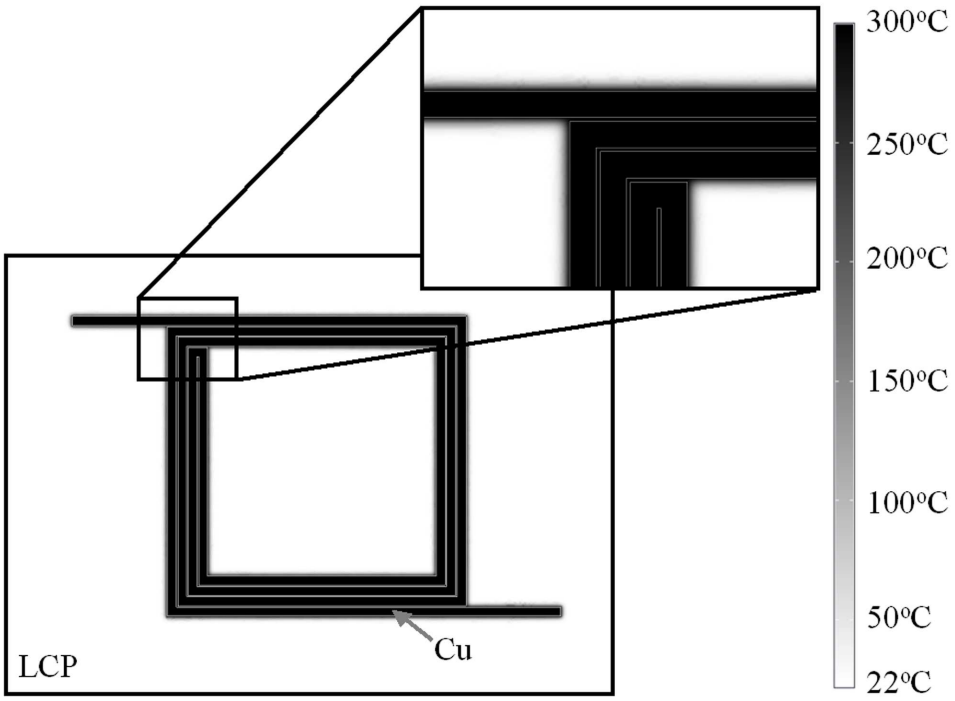

Figure 50: Temperature distribution viewed from top of package

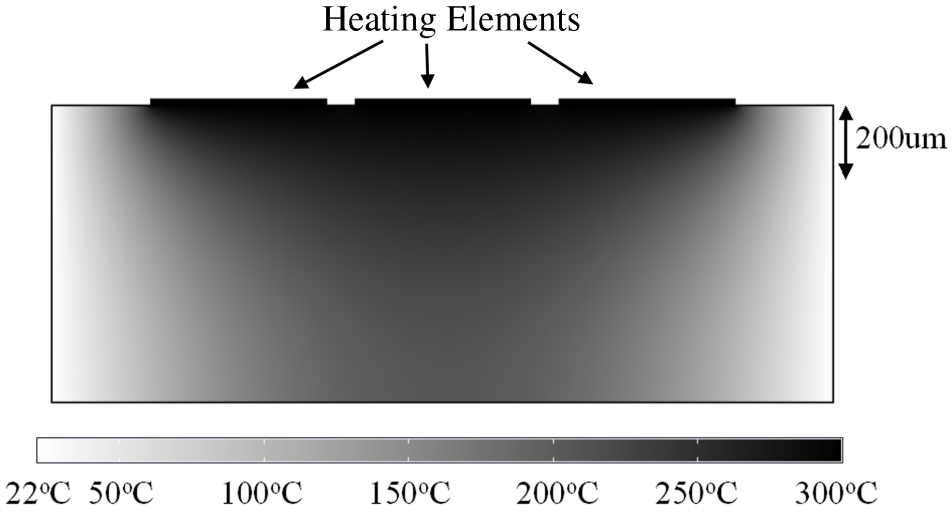

Figure 51: Temperature distribution viewed from side of package

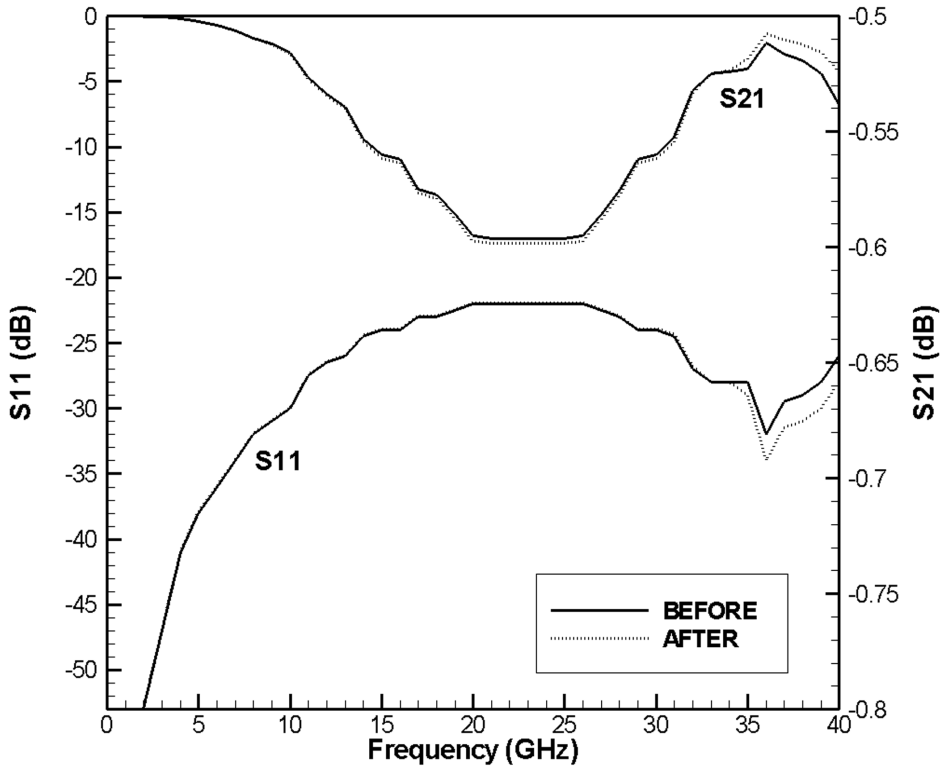

Figure 52: Measurement results of switch before and after water testing in UP (non-actuated) state

removal, the package was peeled apart and the switch was measured a second time. Before and after measurements can be seen for the up (non-actuated) state and the down (actuated) state in Figs 52 and 53 respectively.

The switch exhibits 0.5–0.6 dB loss in the up state, that includes 1 cm of line loss for the CPW line. Return loss in the up state is better than 20 dB for 2-40 GHz. In the down state, the switch maintains isolation better than 20 dB for frequencies > 15 GHz.

No appreciable difference in RF performance was observed in before and after measurements, indicating that no water was introduced to the internal packaged cavity during water submersion.

To test the impact of the bonding method on RF performance, an FGC line was measured before and after bonding. The after measurements were taken with the heating lines removed post-bonding, leaving the seal intact. Fig. 54 shows very little difference between these two cases, showing the RF impact of the sealing method is negligible.

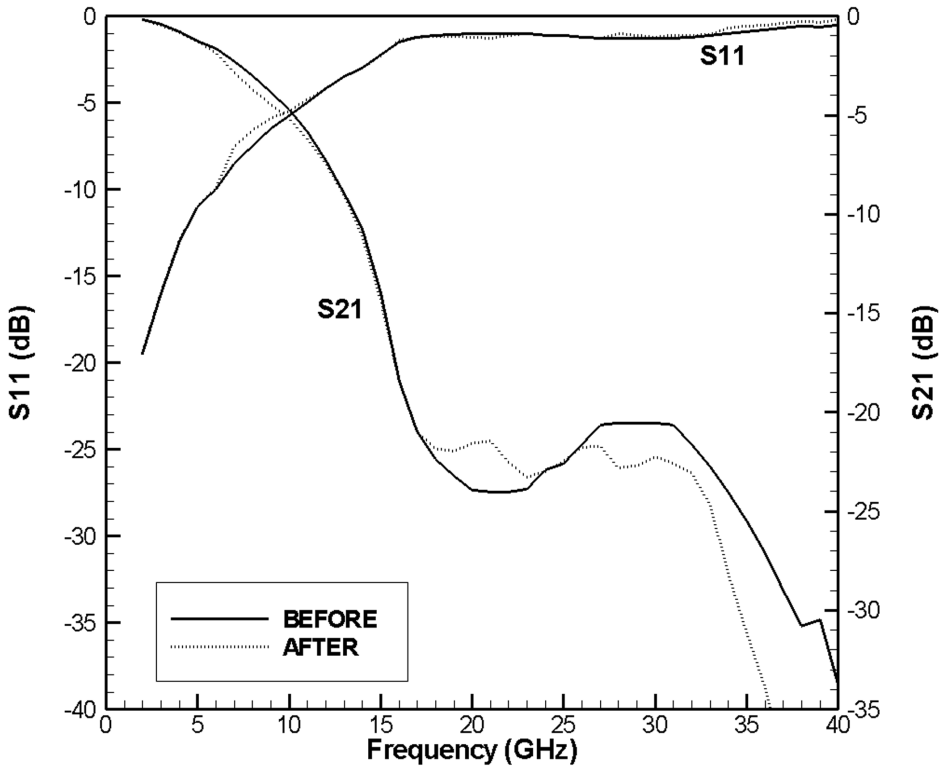

Figure 53: Measurement results of switch before and after water testing in DOWN (actuated) state

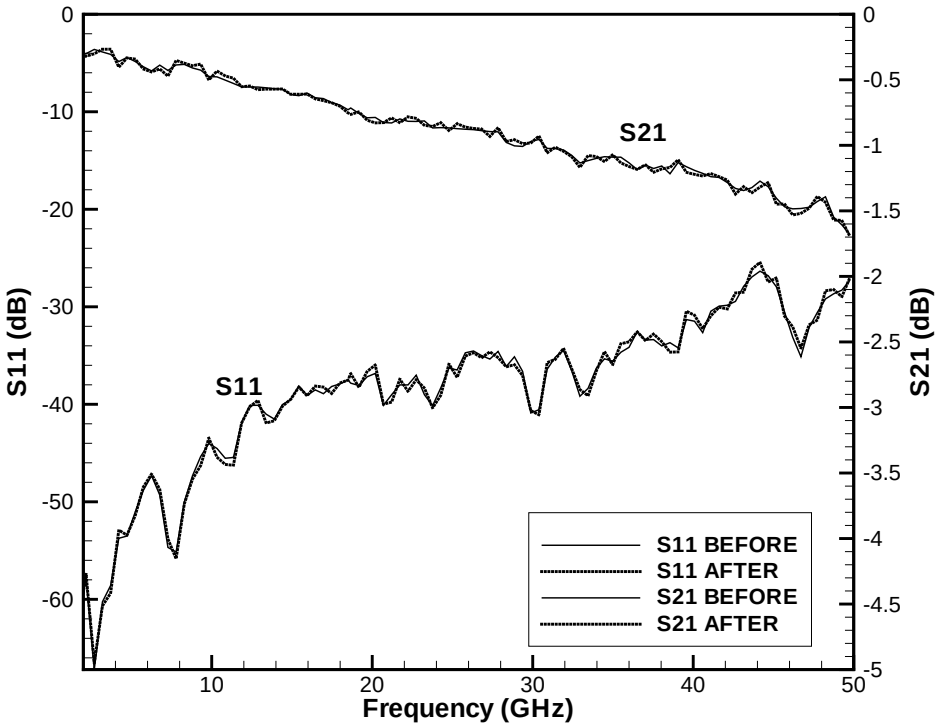

Figure 54: Measurement results of FGC line before and after bonding with heating lines removed.

6.2.4 Conclusion

A low cost localized heating method for LCP using the provided copper cladding has been shown for the first time. Simulations of the heating element structures were performed to examine the thermal characteristics of the bonded regions and switch. Heating lines were fabricated on LCP requiring only one photolithography and etch step, and the MEMS cavity is formed with two 1 mil layers of low-temperature LCP that were etched with a CO_2 laser system. The layers were bonded with localized-heating by passing 7 A of *DC* current through the heating element while compressing the 4 layers together. The seal quality was tested by submerging the packaged switch in 60°C water for 24 hours. Measurements after soaking indicate the bonding technique is successful.

This bonding method provides a very low cost solution to packaging temperature sensitive devices such as the capacitive membrane RF MEMS switch. Unlike previous attempts at localized heating, the easy removal of all heating line metal removes the RF degradation associated with the heating lines, leaving only high performance LCP. This eliminates the

need to tailor transmission lines to widely different impedances that are seen with alternative bonding approaches. Hence, this work improves upon the method shown in [8] by packaging a MEMS device without degrading the RF performance. Due to the minimal impact on RF performance, ease of scalability, versatility and low cost, this bonding method is an ideal solution to packaging MEMS devices in such high-performance polymers as LCP. However, thermal compression bonding remains the technology of choice for applications involving silicon and GaAs substrates.

CHAPTER VII

MEMS-BASED HIGH-PASS/LOW-PASS PHASE SHIFTER

As demonstrated in previous chapters, the High-Pass/Low-Pass phase shift topology is ideal for the broad bandwidth and small size required for monolithic T/R modules. Numerous X-band phase shifters have been demonstrated on SiGe with extremely low phase error and large signal performance. However, each of these suffered from the same setback - insertion loss. While amplifiers can be used in the signal path without significant increases in die-space or power requirements, the overall impact on T/R system noise figure leaves much to be desired.

The largest component of this loss comes from the switches, that have an insertion loss on the order of 1.4 dB each. With 10 switches used in the signal path of a five-bit phase shifter, this loss can add quickly. The ability to utilize pin diode switches instead of MOS-based technology would allow for a potential 0.5 dB decrease in loss per switch (5 dB total). However, this increases the cost of fabrication, and for many technologies is not an available option.

MEMS switches, as seen in a previous chapter, can provide the low insertion loss desired for this application. In addition to extremely low loss, MEMS have an inherently higher IIP_3 and P_{1dB} [3, 46, 53, 73, 81]. This enables higher signal power levels to be handled and maintained, reducing the noise and signal power burden on the rest of the T/R system.

This chapter will examine the use of MEMS switches in place of MOS or HBT devices for the High-Pass/Low-Pass topology. While there has been much research in recent years with MEMS-based phase shifters using various delay line variants [4, 23, 37, 38, 45, 61, 63, 75, 80], this research will provide the first look at the performance of a MEMS-based High/Low-pass approach. With smaller die-area and greatly increased bandwidth possible, using MEMS devices has the potential to significantly reduce the insertion loss of this topology.

7.1 Simulations

Simulations were performed with Agilent Momentum and Ansoft HFSS. HFSS was only used to model the via structures and packaging interconnects because of their 3D nature. To reduce simulation times for the complex bit structures and their interaction, a hierarchy of models was designed and simulated in the 2.5D environment of Momentum.

Circuit level schematics using basic models for spiral inductors and MIM capacitors were used, and their physical parameters optimized to provide the proper phase shift, match, and largest bandwidth. These parameters were used as a guide to develop air-bridged rectangular spiral inductors and MIM capacitors with routing lines in Momentum. Full wave simulations were performed at this filter level with manual changes in component structures until the simulations matched the ideal circuit models as closely as possible. Great care was taken to keep the device dimensions to within fabrication tolerances, with the following self-imposed design rules:

- 50 Ω lines have a width of 20 μm
- The minimum feature size is 3 μm
- The minimum lateral spacing between metals on any layer is 5 μm
- The minimum width of any line longer than 20 μm is 5 μm
- Because of the cost of masks, only 90° angles may be used
- No metal layer can exist above or within 10 μm to a plated line without an underlying sacrificial layer
- The sacrificial layer must extend laterally from its intended location by at least 10 μm
- Vias must be located at least 10 μm away from any metal structures not used specifically to connect the via
- The minimum via dimension is 10 μm

- Any via with a width less than 30 μm must have a length of 50 μm or greater
- plated metals must not exceed 2 μm in thickness
- Silicon Nitride layers must overlap electrode metals by at least 5 μm
- The minimum air-bridge dimension is 10 μm

This put strict limits on the realizable device sizes, but provided a topology that had the highest chance of surviving the fabrication process intact with minimal degradation from a multitude of potential sources:

- Limited alignment accuracy
- Purely anisotropic metal and dielectric etching capability
- Pattern deformation during photoresist reflow and cure
- Non-ideal resist coverage from large discontinuities in surface depth (via depth $>$ 3 times resist thickness)
- Diffusion during exposure in alignment step because of surface micromachined structures
- Plasma back-deposition
- Equipment performance variability

Full wave simulations were performed for each full bit with adjoining MEMS switches (Fig. 55), and the s-parameters were stored for each signal path case in individual files. Once fully optimized, the entire phase shifter was simulated in circuit mode by using the s-parameters from the individual bit sections and manually switching the cases. This provided an accurate simulation of the full phase shifter in less than 2 hours per bit case. The four potential topologies for both the four-bit and packaged five-bit phase shifters took a total of 385 hours using this method.

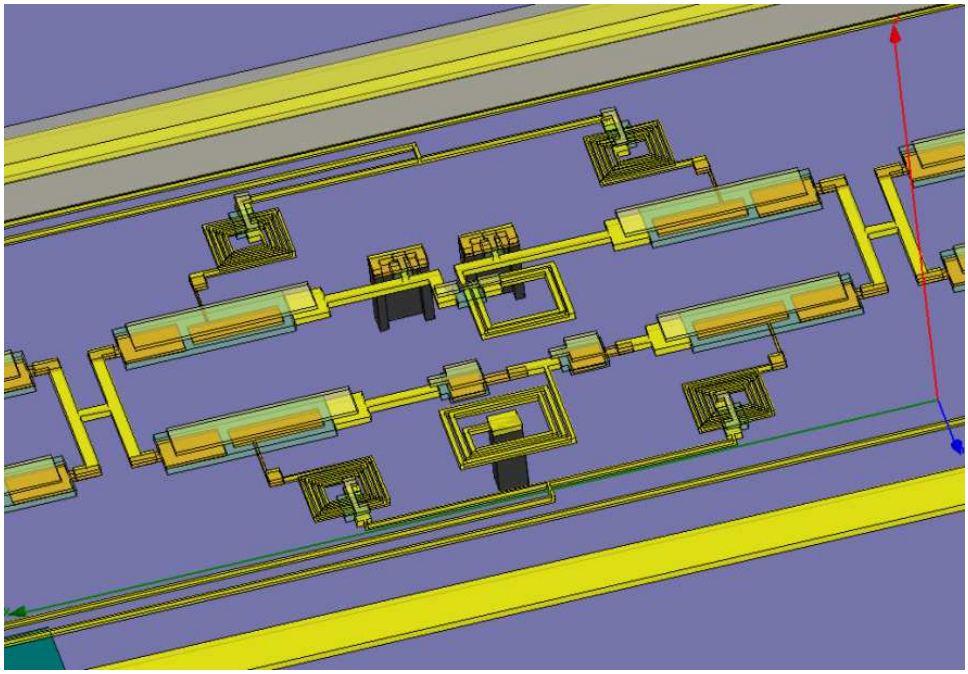

Figure 55: Simulation model for a single bit.

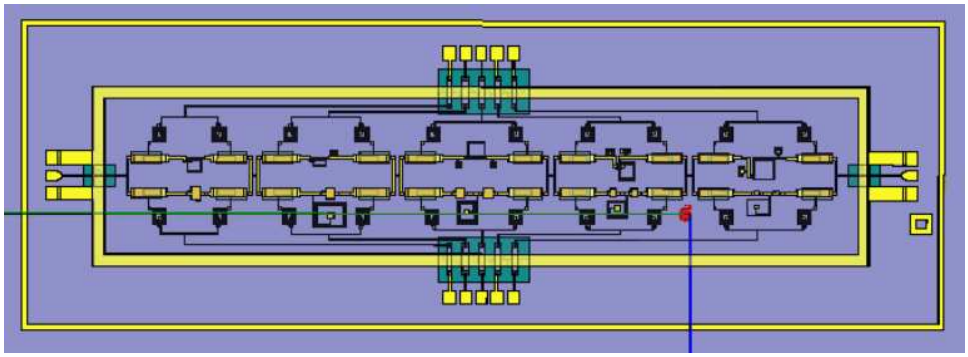

Figure 56: Simulation model for the full phase shifter.

To verify the modular simulations were capturing the bit interaction properly, a few full wave simulations of a full phase shifter were performed (Fig. 56). These simulations took over three days each, so full wave simulations for each phase state and each topology would be impractical. The test cases from the full wave simulation are shown as S_{21} and S_{11} in Figs. 57 and 58 respectively.

Taking metal loss, surface roughness, and dielectric loss into account, the full five-bit shifter showed:

- 2.5 dB loss for 8 - 11 GHz

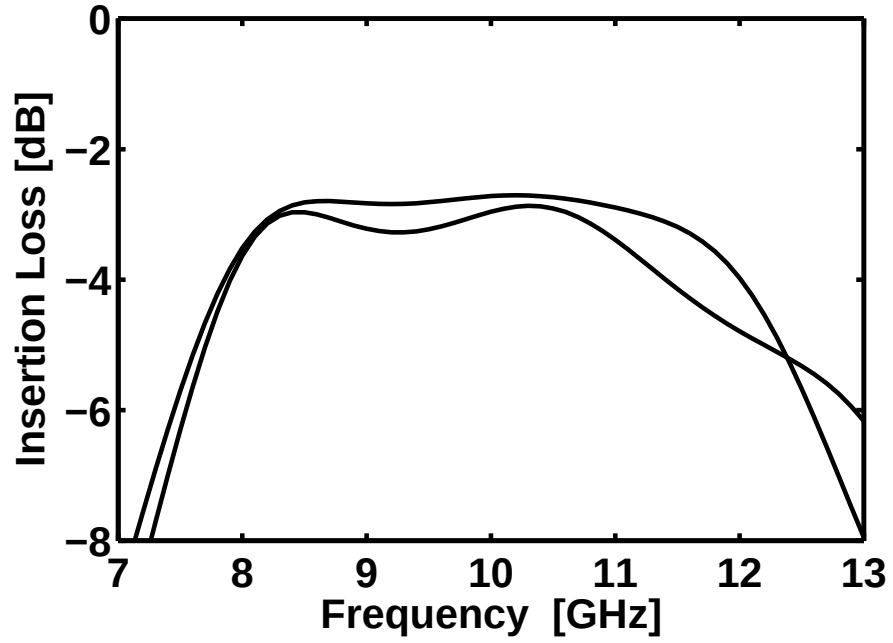

Figure 57: Simulated insertion loss of a few states in the full-wave model of the five-bit phase shifter.

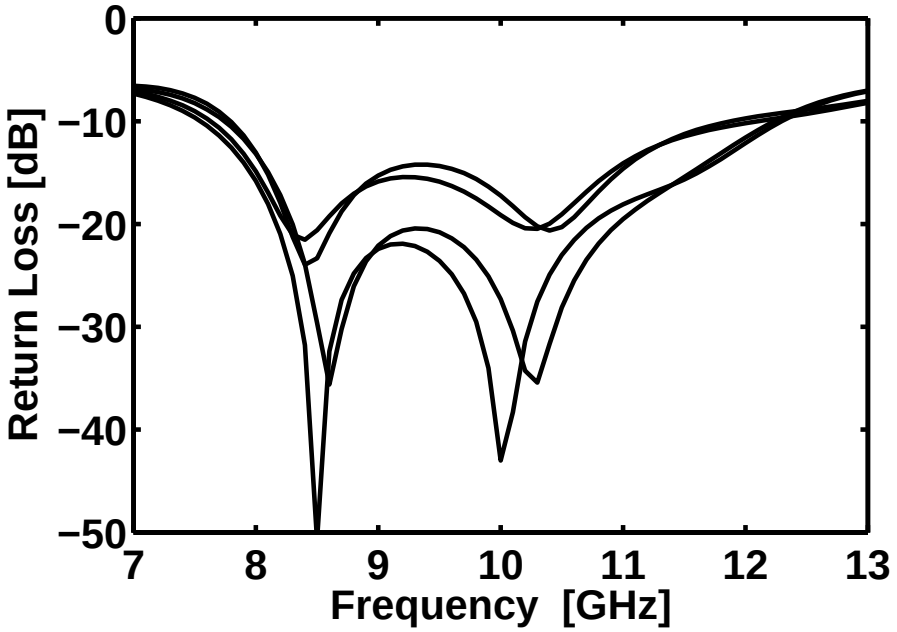

Figure 58: Simulated return loss of a few states in the full-wave model of the five-bit phase shifter.

- $<$ -15 dB reflection
- RMS phase error $< 4^{\circ}$

7.2 Fabrication

The wafer used for the base platform of the phase shifter was a 100 mm diamater high resistivity ($\rho > 10k\Omega$) wafer with a thickness of 525 μm. This platform could be essentially any material (glass, silicon, polymer) provided the surface roughness was on the order of 100 nm or less, but the standard high-resistivity silicon wafer was chosen for the following reasons:

- Most machines in the fabrication facility are optimized for 100 mm diameter wafers.
- The mask aligners provide the optimal contact force with 525 μm thick wafers.
- High resistivity wafers have increased durability to survive the temperature and mechanical stresses of a complicated and long fabrication flow.

Despite the relative low cost of alternative polymer technologies (LCP), the complexity of the fabrication process and strict requirements on alignment accuracy (< 1 μm) demanded the more conventional silicon wafer.

Because of the large number of steps required in the process flow, the description has been separated into three parts: the substrate including the ground metallization and via processing, the surface signal and passive component layers, and the top air bridge and MEMS layers.

7.2.1 Substrate: Ground-plane, SiO_2 and Via Process

The ground plane was formed with 1.2 μm of Au using 250 $\AA$ of Ti for adhesion. To achieve the lowest amount of surface roughness, these metal layers are generally deposited using evaporation. However, metal impurities introduced into the crucibles by stray electron bombardment produced a film with randomly distributed carbon molecules. This not only results in higher metal loss, but hinders proper crystal formation for the SiO_2 layer that is deposited on top of the ground layer. This forms both 3-4 μm holes where the carbon

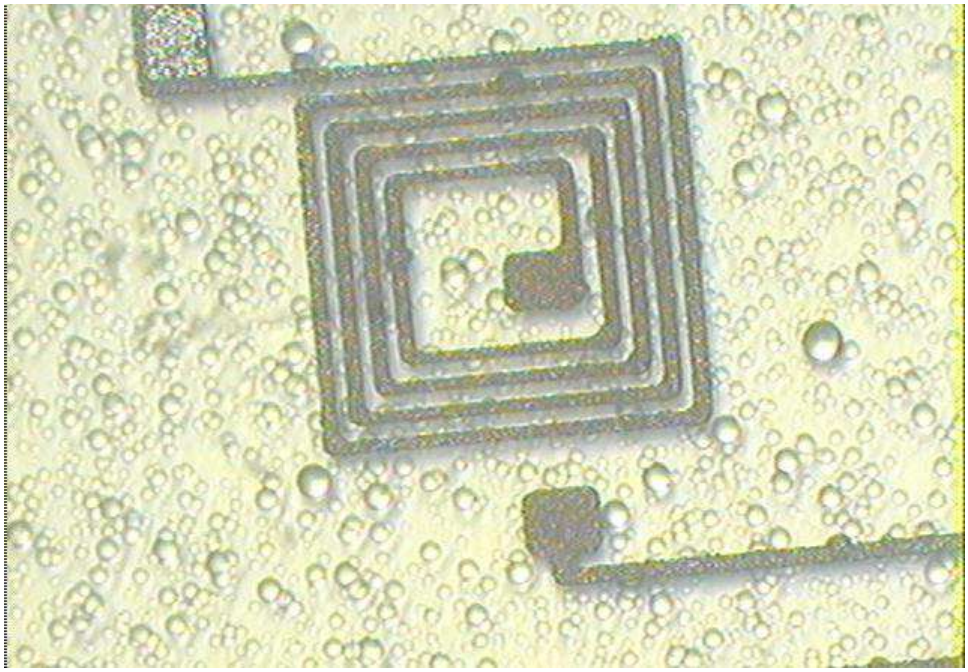

Figure 59: Microscope photograph of damaged SiO_2 substrate.

molecules were located and promotes local delamination of the SiO_2 during the many 200 °C temperature cycles during later process steps. The metal layer was instead formed by sputtering, a process that uses argon atoms to bombard target metals. An example of the damage caused by this oxide problem with metal contamination is shown in Fig. 59.

To simulate a layer stack-up similar to many commercial Si and SiGe processes, a 10 μm SiO_2 layer was used as the primary substrate. This was deposited at 250 °C by plasma enhanced chemical vapor deposition (PECVD) using the Unaxis. Film quality and thickness were verified with the Nanospec optical refractometer.

Chrome was then sputtered to a thickness of 1 μm to use as a mask for the via etching process. This chrome mask was patterned using SC-1827 and chrome etchant (ceric ammonium nitrate and nitric acid).

Because the sample contained metal, the STS AOE (Advanced Oxide Etcher) was used instead of the standard etching process in the PlasmaTherm ICP. This required mounting the prepared sample to a 150 mm diameter wafer using Crystal Bond, a thermal mounting polymer. A high-temperature formulation was used to allow the helium cooling system on the STS AOE to keep the chrome layer from delaminating from the intense heat generated

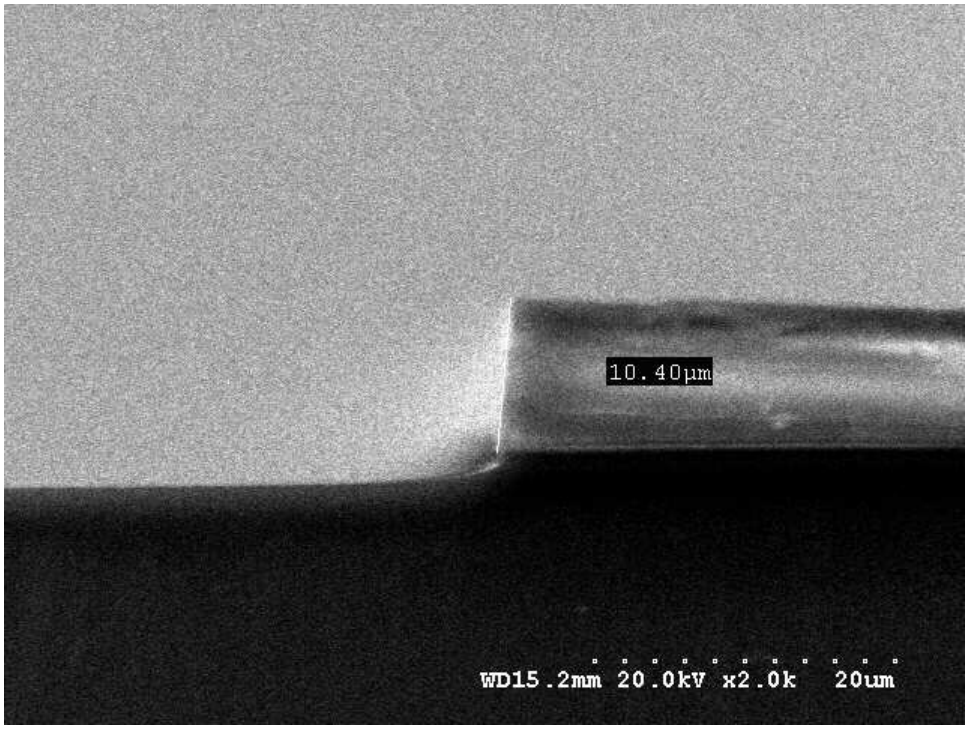

Figure 60: Scanning electron microscope picture of via cross section.

by the inductively coupled plasma. This was applied to the 150 mm mount wafer that was heated to 95 °C. The 100 mm sample was pressed on top and manipulated laterally to ensure full contact without voids. The mounted sample was then cooled to room temperature, with excess bonding compound removed with a razor blade.

The sample was etched with a 1800 W plasma, requiring only 24 minutes to etch the 10 μm vias. Removal of the mount wafer was done mechanically after reheating to 95°C, and the boding polymer was removed with an acetone bath. Plasma etching often leaves a thin layer of oxide on metal surfaces because of back-deposition, so a 30 second rinse in buffered oxide etchant (30% ammonium flouride, 10% hydrogen flouride, 60% deionized water) was performed. Chrome etchant was again used to remove the remaining metal mask.

To check the quality of the via etch with the STS AOE, a sample was diced and examined with a scanning electron microscope (Fig. 60).

7.2.2 Signal Routing and Passive Components

The next step in the process flow is to simultaneously electroplate the vias, primary signal lines and inductors with gold. Because of the depth and high aspect ratio of the vias, the metal seed layer must be deposited isotropically. This was achieved by sputtering Ti/Au/Ti with thickness of 200/2300/200 $\mathring{A}$.

The electroplated pattern was formed with SC-1827, and the exposed top Ti layer removed with hydroflouric acid. The exposed patterned gold was plated to a thickness of 1.5 μm in a 55 °C potassium aurocyanide solution. Plated metal thickness was determined by before and after profilometry scans with the Tencor P15 profilometer, measuring the decrease in photoresist patten depth.

Photoresist was then removed with an acetone bath, and the top Ti seed layer was again removed with hydroflouric acid. However, instead of removing the remaining seed layers, the thin gold layer was used to create the electrode and bottom capacitor metallization. This was patterned again with SC-1827, and the exposed seed layer was then etched in potassium iodide and finally hydroflouric acid. This left not only the 1.5 μm plated vias, signal lines and inductors, but also the 2300 $\mathring{A}$ gold forming the MEMS electrodes and bottom plates to all of the capacitors.

This thin gold layer is required as the 2000 $\mathring{A}$ SiN layer used for the capacitor dielectric and MEMS *DC* blocking dielectric is prone to edge effect. The crystal structure is unable to properly form on the edge of a metal step, leading to a short in capacitors or the electrode of the MEMS. Using a metal layer with a thickness on the same order as the SiN prevents this from occurring.

The 2000 $\mathring{A}$ SiN layer is deposited by PECVD again with the Unaxis. Thickness is verified with the P15 profilometer, since the large number of dielectric and metal layers beneath the SiN layer difficult to examine with refractometry. Patterning is accomplished with SC-1827 and etching with the PlasmaTherm RIE (reactive ion etcher) using SF_6.

7.2.3 MEMS Membranes, Inductor Air-bridges and Capacitors

Once the sample has reached this stage in the fabrication process, only the top metal layer remains. This defines the membrane used for the MEMS switches, the air-bridges used to connect the internal and external lines of the inductors, the top plates to the capacitors, and connects to the plated signal lines from the previous step.

Aluminum was chosen for this metal layer for two very specific reasons: its much lower Young's modulus allows for significantly reduced MEMS activation voltages, but more importantly, it allows the top layer to be completely removed and refabricated without causing damage to previous layers in the event of a failure during the final process steps. The common failure mechanisms will be discussed when the corresponding process step is presented. All previous layers were purposefully fabricated with materials that are relatively inert to the weak aluminum etchant ($HCl:HNO_3:H_2O$), so problems with the remaining steps would not necessarily require a new sample to be started from scratch.

While the metal for the top layer of the capacitors rests directly on the sample, the air-bridges for the inductors and the MEMS membranes are suspended above the sample. This is achieved by spinning SC-1827 at 4000 RPM, that after photolithography creates a pattern with a thickness of 1.4 μm. The sample is then baked on a hot plate for 2 minutes at 120 °C to allow for reflow. This causes the high aspect ratio of the edges of the patterned resist to reflow a small amount, slightly reducing the pattern definition but also causing the edge to soften enough to accommodate an anisotropic metal deposition. Without this reflow it is possible the metal deposited on top of the resist would not make contact with the metal on the substrate.

Because the resist is likely to experience high temperatures during the final metal evaporation, the sample is then cured at 140 °C on a hot plate for 15 minutes, followed by another 15 minutes at 140 °C in an oven.

Metallization is performed by evaporation with an electron beam evaporator using a water cooling system to keep the sample as cool as possible. Sputtering is a much lower temperature method, but the impact of the metal molecules causes the metal layer to protrude into the sacrificial layer making resist removal impossible. First a 150 $\mathring{A}$ Ti layer

is evaporated at a slow rate of 1 $\mathring{A}$/s, followed by a 1 μm Al layer at a rate of 1.5 $\mathring{A}$ with 20 minute rest periods every 3000 $\mathring{A}$. If the temperature of the resist sacrificial layer rises above 150 °C, it will bubble causing significant damage to the metal layer above it.

Once deposited, SC-1827 is again spun to define the top metal layer. The final sub-micron alignment is difficult to achieve, as the alignment marks are covered by the 1 μm Al layer and the additional height of the sacrificial layer causes a slight amount of diffusion. Generally, the alignment before the final etch can not be verified to better than an accuracy of about 4 μm.

After patterning, the aluminum is etched in aluminum etchant heated to 50 °C. Here it is possible that the very small capacitor tops ($< 10\mu$m) are damaged because of reactive impurities in the aluminum, or weakly defined photoresist from diffusion caused by the slight sample-mask separation is unable to protect the metal layer. If this step is successful, the remaining thin Ti layer is removed with hydroflouric acid.

To remove the sacrificial layer and top metal resist, the sample is submerged for 12 hours in SC-1112A photoresist stripper. SC-1112A is generally not used with organic polymers (LCP) as it is a much harsher formulation that can cause damage to organic materials. The SC-1164 stripper more commonly used to remove the sacrificial layer would require approximately 24 hours to fully remove the resist, but would also damage the very reactive aluminum membranes.

The sample is then carefully transferred to deionized water for a few minutes to remove the SC-1112A, and then transferred to an isopropyl alcohol bath.

For the final step, the sample is dried in the Tousimis Super Critical Dryer. This introduces CO_2 gas into the chamber, and changes the pressure and temperature of the chamber to create a condition where the surface tension of the isopropyl alcohol is zero. The isopropyl alcohol is then replaced with CO_2 gas, and the chamber brought back to ambient temperature and pressure.

If after drying the sample has the top metal layer intact without damage from a distorted sacrificial layer and is in proper alignment, it is complete and ready for measurement. Otherwise, the top metal layer is removed and this section of fabrication is repeated.

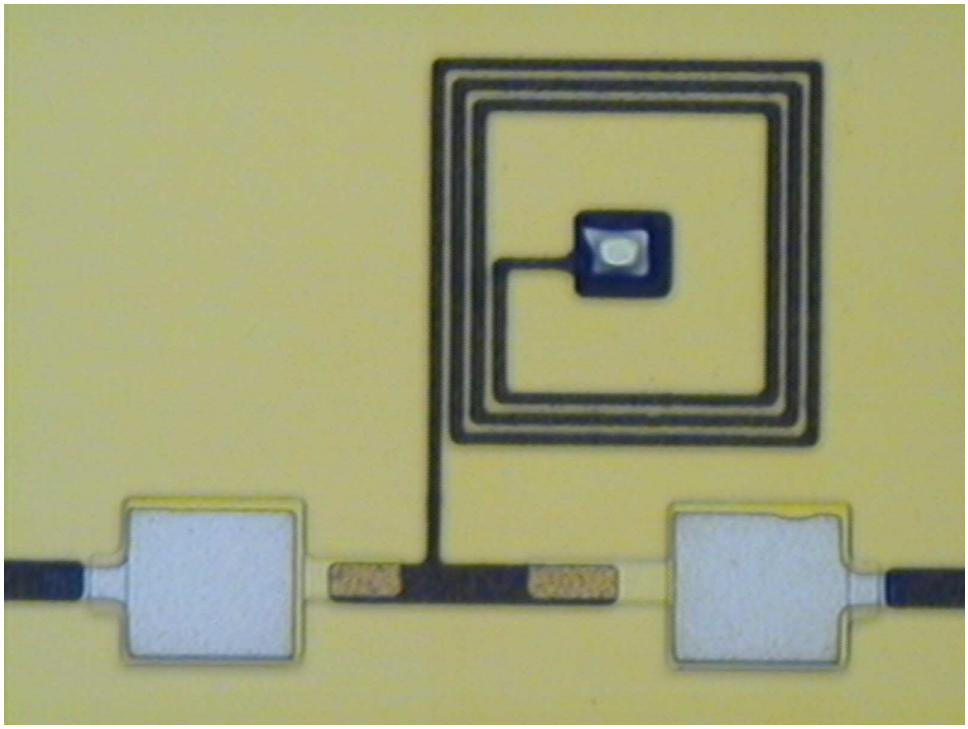

Figure 61: Microscope photograph of a single filter section in the High-Pass/Low-Pass phase shifter showing series MIM capacitors and a shunt spiral inductor with a central via to ground.

Microscope photographs of filter sections and bits can be seen in Figs. 61–63. The vias for the small shunt capacitors in Fig. 62 wrap around the capacitor in the shape of the letter C. This was done to increase the total area of the via to increase the probability of a successful etch and reduce resistive losses in the via metallization.

7.3 SPDT MEMS Switches

Insertion and return loss for the MEMS switch in the on- and off-state are shown in Fig. 66. The MEMS switch demonstrates a loss less than 0.2 dB for 8–12 GHz, with an isolation better than 18 dB. This high isolation was achieved in part by a slight curling of the long membrane, evident by the gradient in light reflection on the membrane in Fig. 64. Curling in this case is caused by stresses induced in the membrane by differences in CTE between the 1 μm thick Al top layer and the 200 $\AA$ Ti layer used for adhesion, that remains underneath all Al structures. Because of the low Young's Modulus of Al, the curling produces only a slight increase in actuation voltage, that for this switch is 22 V.

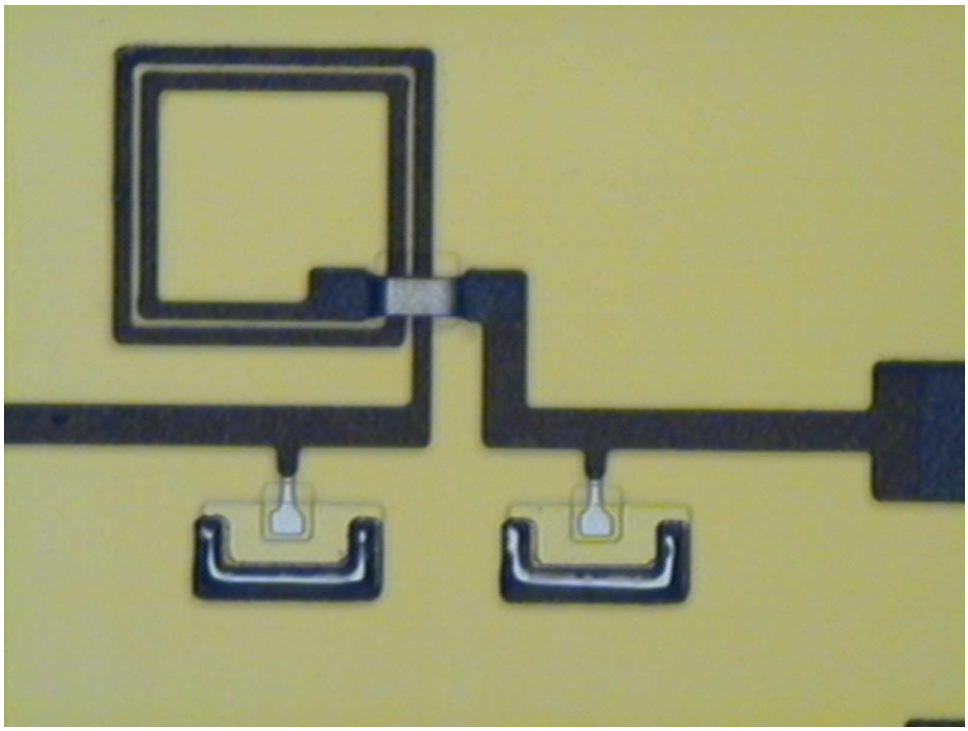

Figure 62: Microscope photograph of a single filter section in the High-Pass/Low-Pass phase shifter showing a series inductor with an aluminum air-bridge connection and shunt MIM capacitors with vias to ground.

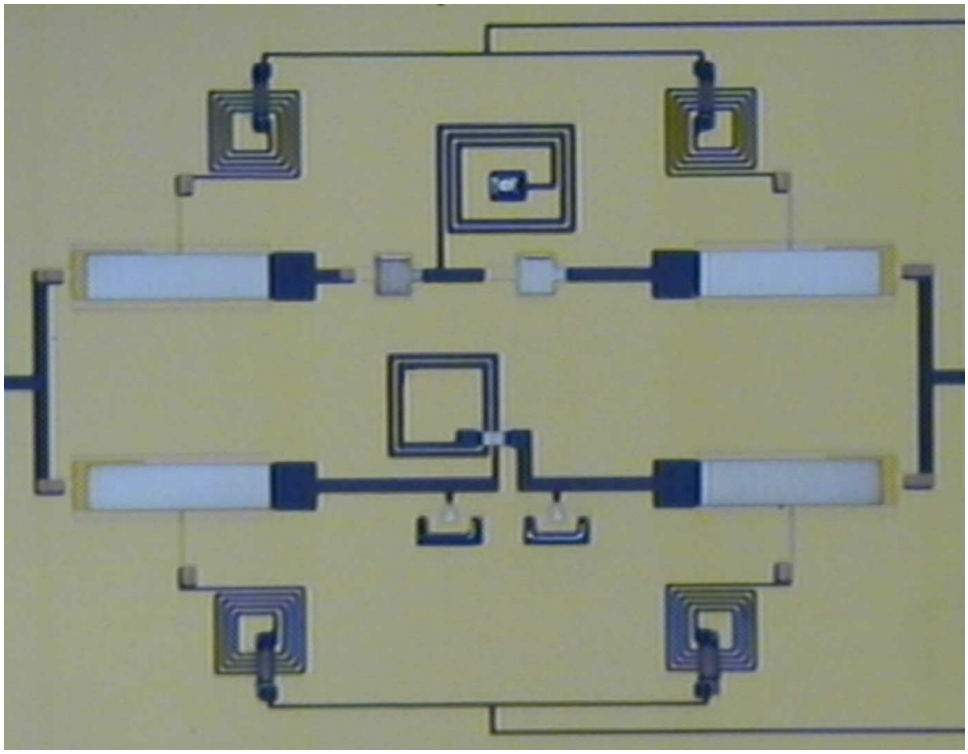

Figure 63: Microscope photograph of a single 45 degree bit.

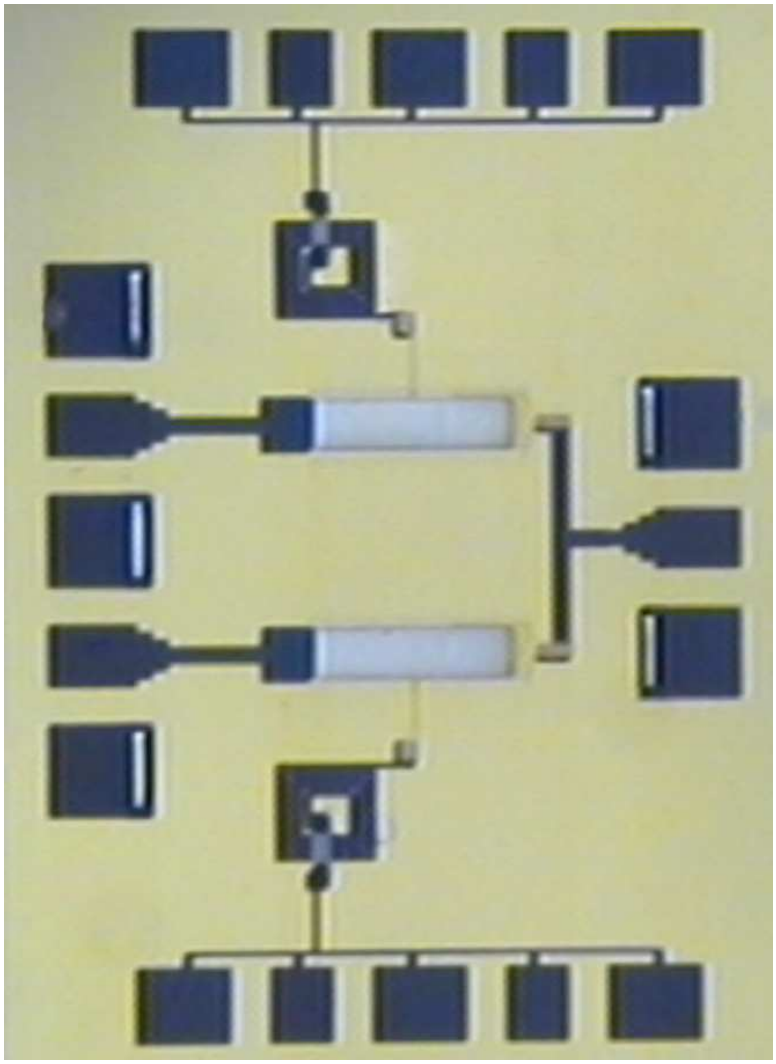

Figure 64: Microscope photograph of a single-ended SPDT MEMS switch.

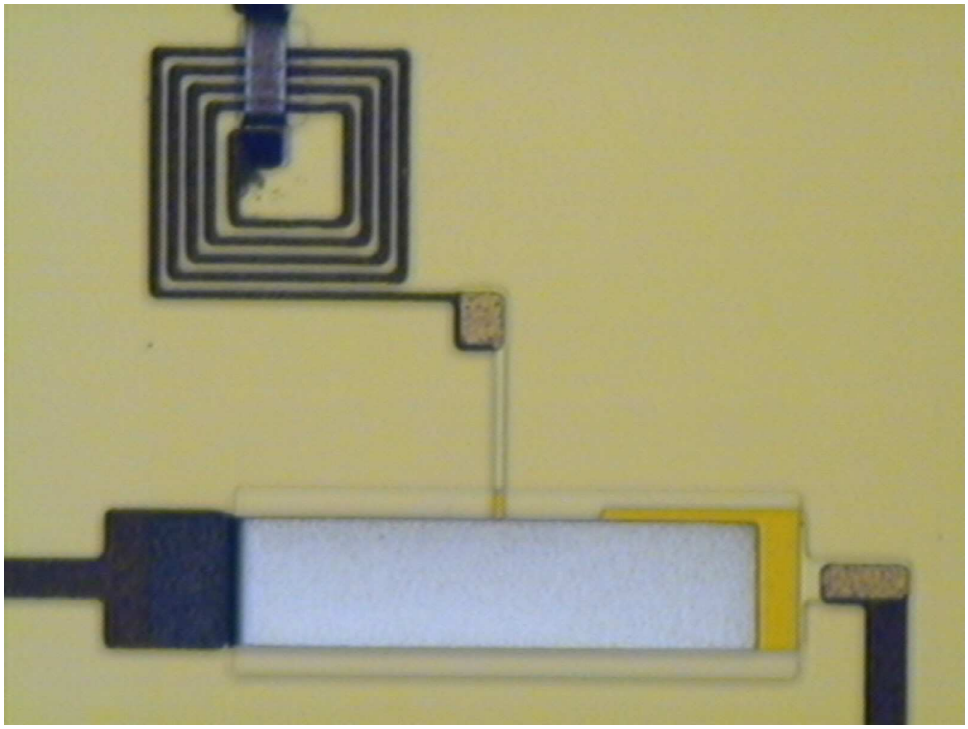

Figure 65: Close-up microscope photograph of a MEMS switch.

The return loss in the on-state is better than 16 dB over the band of operation. For the four-bit phase shifter, total switch loss accounts for approximately 1.6 dB. This is slightly more loss than a single switch in the SiGe MOS phase shifter, showing the clear advantage MEMS has over active switches in terms of insertion loss.

7.4 Four-bit MEMS Phase Shifter Measurements

The full four-bit MEMS phase shifter (Fig. 67) was configured in a $180° - 22° - 90° - 45°$ bit order to keep bits with the least loss separated. This provides a slight decrease in phase error from fabrication tolerances by attenuating reflected power from mismatched lower shift value bits [48]. Because simulation models for the inductors were less accurate than that of the MIM capacitors, the hybrid pi/t topology was used. This also provides a significant reduction in the die-area required as the number of inductors and the space required to minimize inductive coupling is reduced [47].

At 5.5 mm long and 1 mm wide, the full four-bit shifter has a die area of only 5.5 mm^2. This small size is particularly evident when compared to the 4.3 mm length required for a

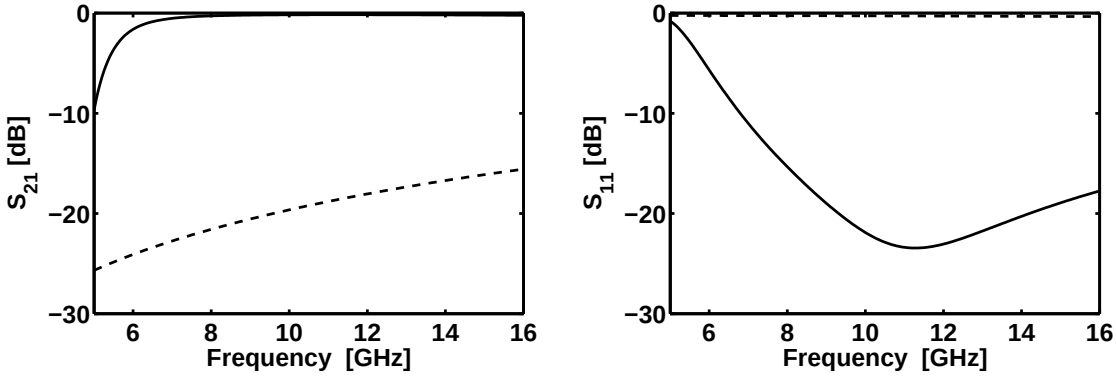

Figure 66: MEMS switch measurements.

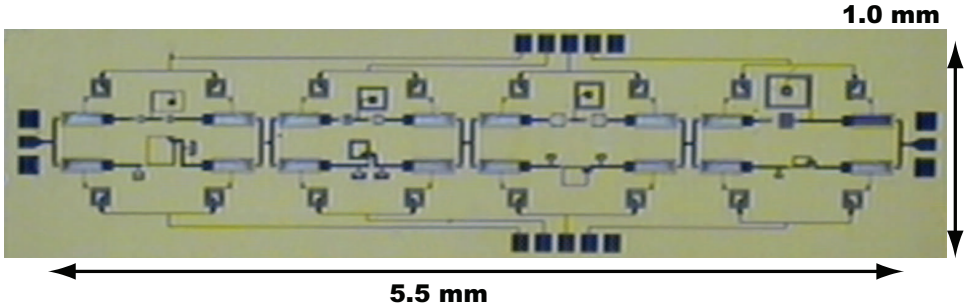

Figure 67: Microscope photograph of the full four-bit MEMS phase shifter.

single 90° delay line in a transmission line based phase shifter.

Each bit contains both a high-pass and low-pass filter section, with MEMS switches on either side to select the desired signal path. Because the switches on either side of a filter section will both be activated or deactivated at the same time, the bias lines for both switches are tied together. This occurs on the DC side of the 3 nH choke inductors to minimize coupling.

The bias lines are routed to a group of DC pads with 150 μm spacing to facilitate DC probe cards to be used to simply measurements (Fig. 68). A total of 8 DC lines are required to operate the 4 high-pass and 4 low-pass switch groups, with pads located on the top and bottom of the phase shifter. Active lines were tied together at a 25 V source, and connected manually to provide measurements for all 16 phase states. A photograph of the measurement setup is shown in Fig. 69.

Measured return loss and insertion loss for the four-bit MEMS phase shifter can be seen

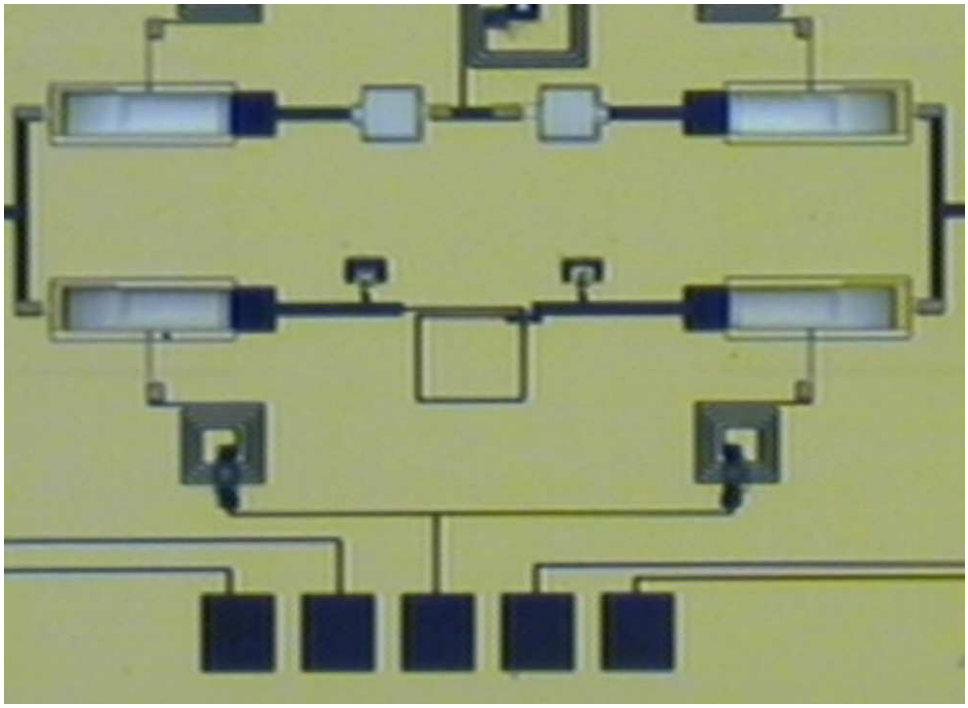

Figure 68: Microscope photograph of *DC* bias pads used in the four-bit MEMS phase shifter.

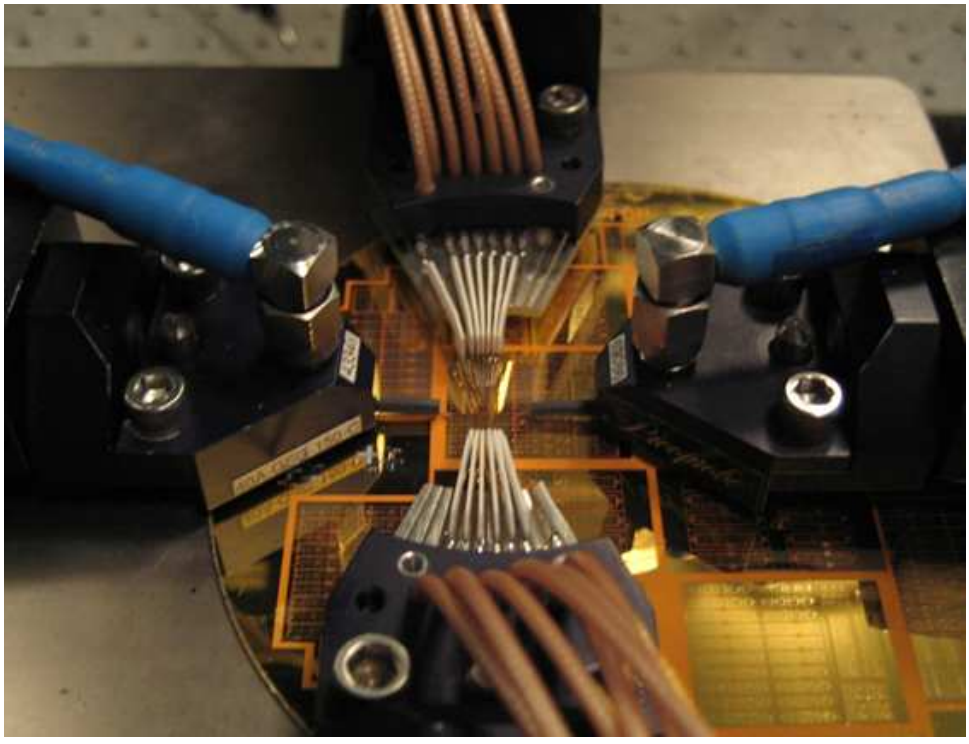

Figure 69: Photograph of measurement setup showing *RF* and *DC* probes.

in Figs. 70 and 71, respectively. The phase shifter maintains a return loss better than -11 dB for 8-12 GHz, with an average loss of 3 dB. The maximum loss is 4 dB at 8 GHz, with a loss variation of 2 dB across the phase states for all of X-band. This variation in loss is because of the higher amount of loss in the bits with larger inductors.

This inductor loss is a direct result of a thin 1 μm gold plating for the primary metal lines used in the inductor. To accommodate the 5 μm wide line and spacing used in the inductor, a plating method was used that provides the highest degree of resolution for metal thickness above 200 nm. The maximum metal thickness achievable with plating techniques is directly dependant on the photoresist thickness, as the plated metal tends to have preferred growth on the sidewalls of the resist pattern. Because of this, the plated thickness must stay below half the thickness of the patterned resist for feature dimensions less than 20 μm. Diffusion during photolithography exposure limits the photoresist thickness for this pattern resolution to 2 μm, hence 1 μm was the maximum thickness achievable for the inductor metal layer.

Measured phase shift for all 16 states is seen in Fig. 72 with RMS phase error over frequency in Fig. 73. The local minimum in phase for each state was shifted slightly lower in frequency, and the shift was on average marginally lower than simulated. RMS phase error is lower than 7° up to 11.3 GHz, and lower than 10° for all of X-band.

7.5 Four-bit Shifter Performance Discussion

The first MEMS-based High-pass/Low-pass phase shifter has been successfully demonstrated. The circuit can provide 360° of phase shift, with an RMS phase error less than 10° over the entire band of operation. The shifter achieves an average insertion loss of 3 dB, and maintains a return loss greater than 10 dB for all states over the band of operation. Total shifter die-area was 5.5 mm^2, nearly the same as the hybrid SiGe phase shifter presented earlier and significantly less than the all-pi SiGe phase shifter area of 9.84 mm^2.

This is a substantial improvement in the insertion loss over the transistor-based SiGe phase shifters, that averaged higher than 14 dB for the same four-bit topology. Further discussion on the advantages and disadvantages of MEMS and active SiGe will be discussed in a later chapter.

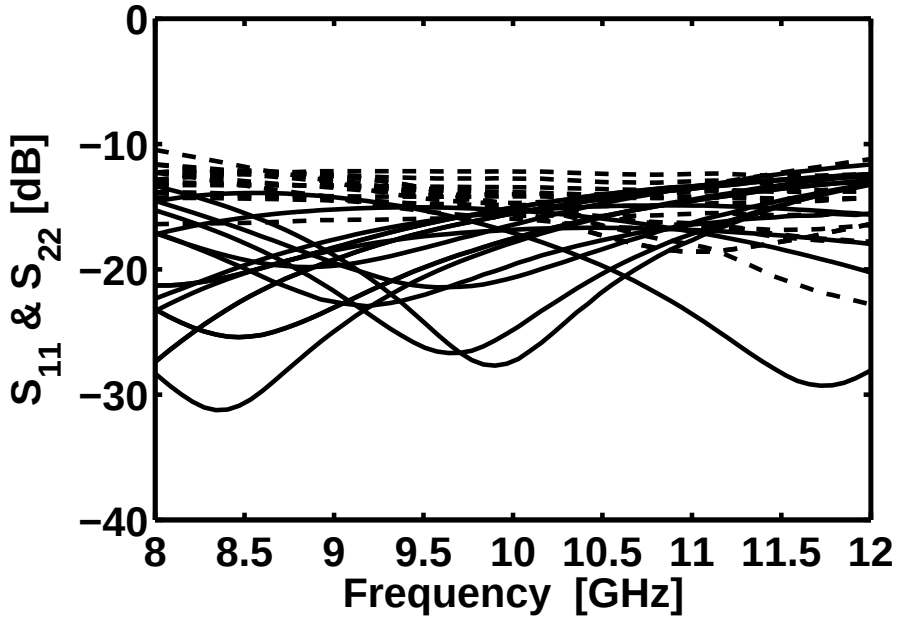

Figure 70: Input and output match for four-bit MEMS Phase Shifter.

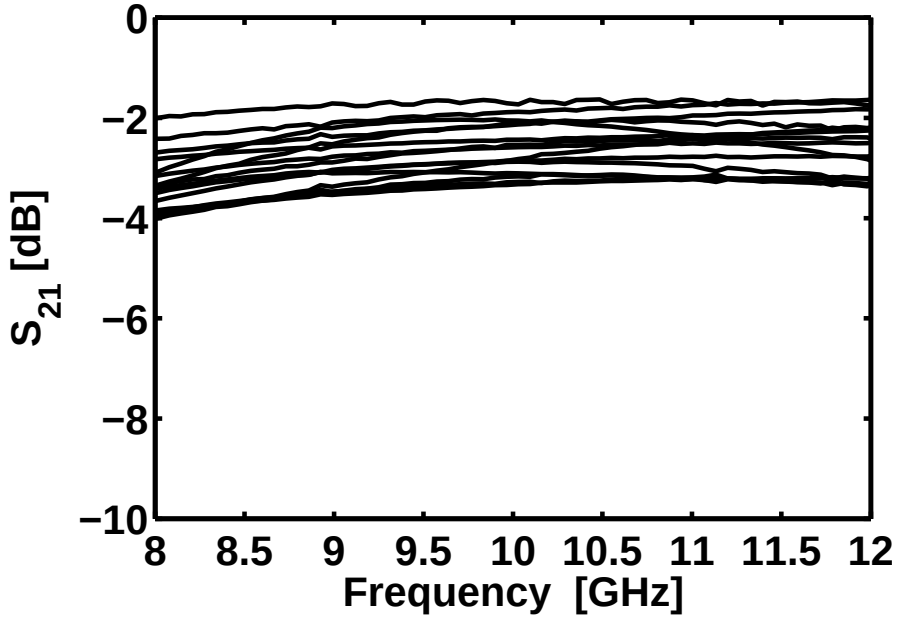

Figure 71: Insertion for four-bit MEMS Phase Shifter.

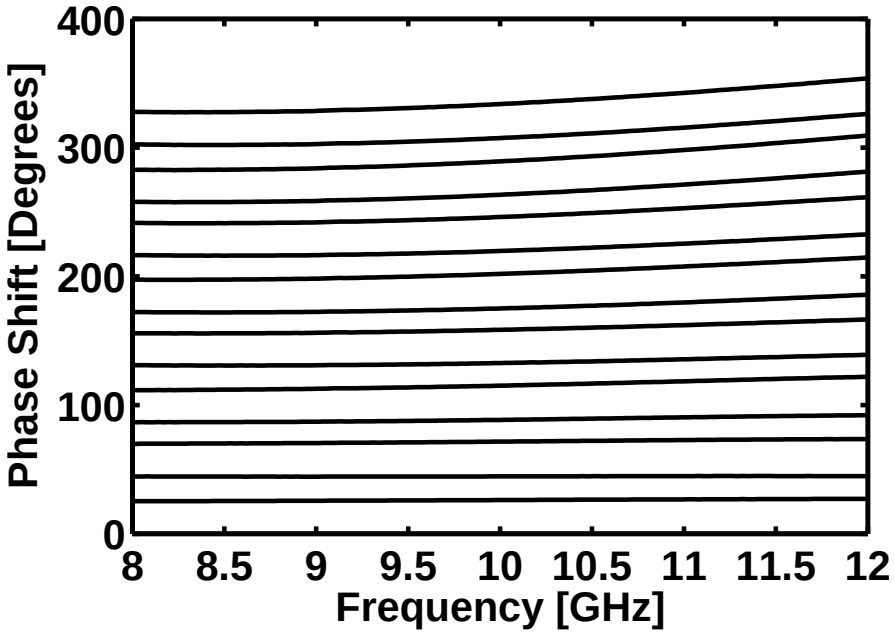

Figure 72: Phase Shifts for four-bit MEMS Phase Shifter.

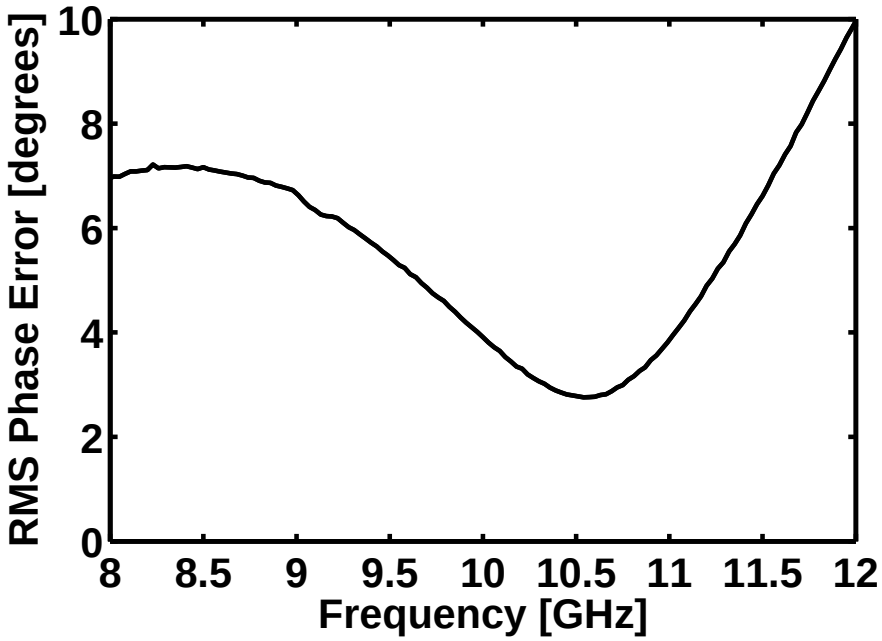

Figure 73: RMS Phase Error for four-bit MEMS Phase Shifter.

7.6 Packaged Five-bit MEMS-based High-Pass/Low-Pass Phase Shifter

The wide-band micromachined packaging method discussed in an earlier chapter will be adapted to the phase shifter topology, requiring both input and output RF interconnects as well as 10 individual *DC* interconnects. This method provides the lowest loss and bandwidth of the alternative popular approaches [2,42,68,76], while remaining a suitable bonding temperature for MEMS devices and leaving the primary sample wafer free of bulk micromachining.

The full five-bit MEMS phase shifter was configured in a $180° - 22° - 90° - 11° - 45°$ bit order to keep bits with the least loss separated. As before, this provides a slight decrease in phase error from fabrication tolerances by attenuating reflected power from mismatched lower shift value bits. The uncertainty in the discrepancy between modeled and actual performance in this case is higher due to an additional bit with a smaller shift value [48]. As such, additional time was spent in simulation to ensure the optimal bit topologies.

7.7 Phase Shifter Package Fabrication

The fabrication process for the packaged MEMS phase shifter is identical to that described for the un-packaged phase shifter, with only two differences. The first is etching the ground plane in the initial steps to provide a space for signal routing, and the second is the simple addition of a bonding ring on the perimeter of the phase shifter that is plated along with the signal lines, inductors, and vias.

The Ti/Au ground plane is patterned with SC-1827 and etched with potassium iodide and hydroflouric acid. This leaves openings in the ground plane in the vicinity of the interconnect, with a metal line passing beneath the bond ring. Vias are etched in later steps, that are then plated to connect the patterned bottom metal line to the surface plated signal lines.

This technique is used for both the RF lines (Fig. 74) and both sets of 5 bias pads (Fig. 75). Scans from the P15 profilometer indicate the surface roughness on the bond ring to be less than 200 nm, which is acceptable for thermal compression bonding.

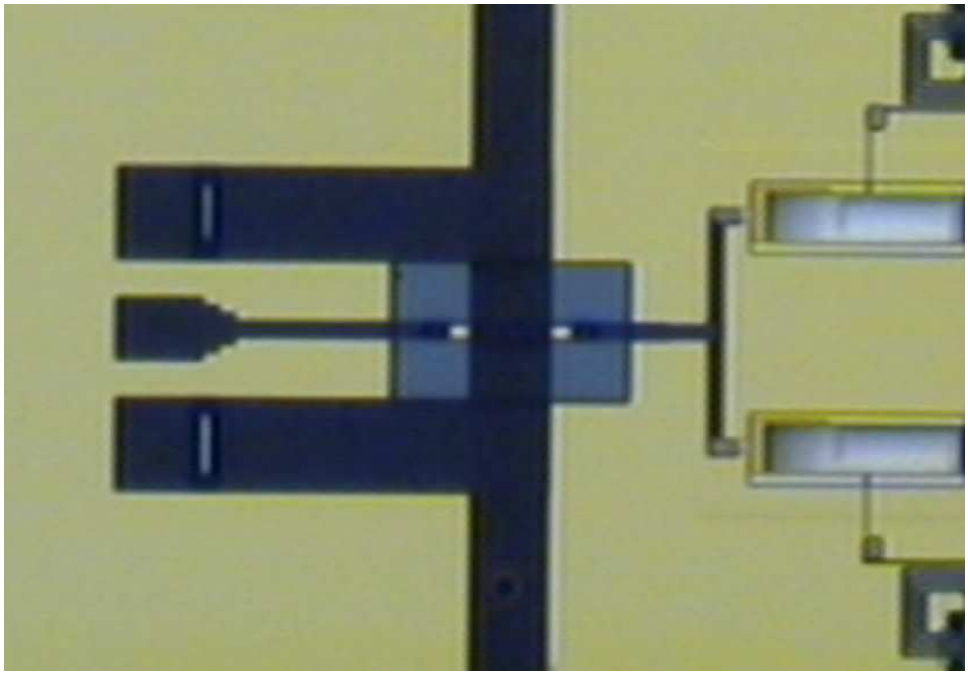

Figure 74: Microscope photograph showing the RF interconnect and bonding ring.

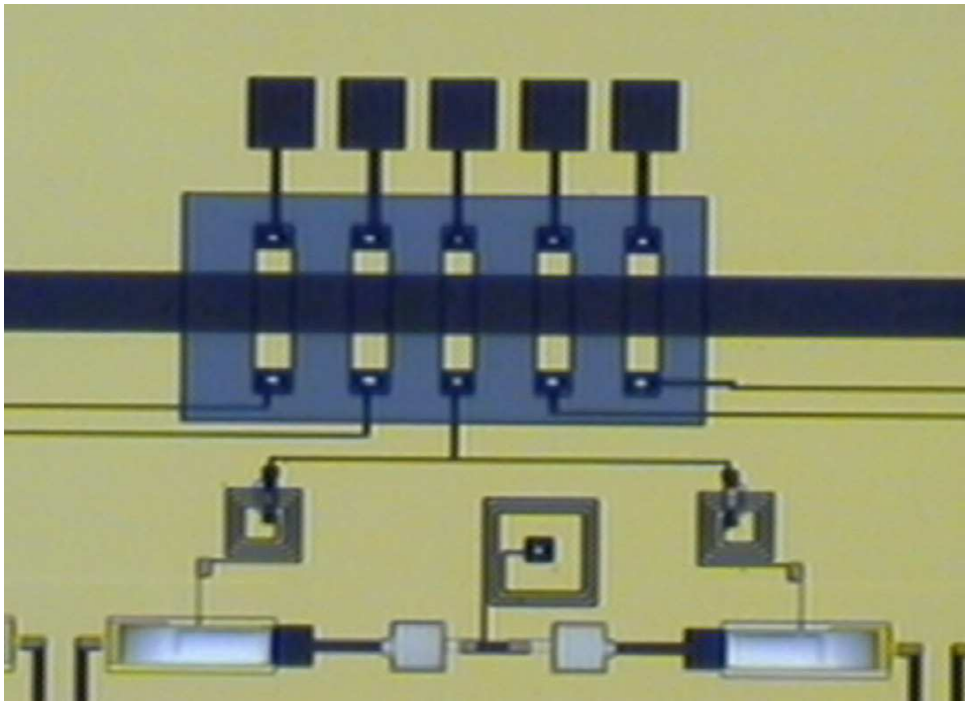

Figure 75: Microscope photograph showing the DC bias interconnects and bonding ring.

The cap wafer is fabricated by bulk micro-machining a 300 μm thick silicon wafer. A 2 μm thick layer of SiO_2 was deposited by PECVD, and then patterned with SC-1827. Because the removal of the patterned oxide determined only the measurement windows that had critical dimensions on the order of a few mm, a 1:1 ratio of hydroflouric acid to deionized water was used in lieu of a plasma etch. A 8 μm thick layer of SPR-220 photoresist was then used to define the bonding ring structures. Both the oxide and resist serve as etch masks for the DRIE step that bulk micromachines the silicon wafer.

The sample is bonded to a 300 μm carrier wafer with cool grease, a low-temperature thermal compound. The higher temperature bonding compound used in the via etching step in the previous chapter could not be used. Bulk micromachining weakens the crystal structure of the silicon wafer and the removal of the higher temperature compound post-processing would destroy the silicon wafer. The much lower plasma power (and as a result much slower etching time) used in the bulk micromaching step makes the cool grease an acceptable mounting option.

The 100:1 selectivity of the Si:SiO_2 and 10:1 selectivity of the Si:resist creates a three-level wafer in a single etch step. The top layer, which is the only original surface, comprises the smooth bond rings that match the bond rings on the MEMS phase shifter wafer. The second level at approximatly 150 μm deep creates the cavity layers that encase the phase shifters after bonding. The third layer is etched completely through the wafer to enable both RF and DC probes to contact the lines on the main wafer for measurement.

Once etched, 2 μm of Au with a 200 $\mathring{A}$ Ti layer for adhesion is sputtered on the cap wafer for eutectic bonding.

7.8 Bonding Process and Quality Testing

A continuous bond ring surrounds the entire five-bit phase shifter, with only the RF and DC bias pads remaining external for measurement purposes (Fig. 76).

Wafer alignment is performed with a Karl-Suss BA6 wafer aligner. Bonding is achieved by ramping the temperature to 200° C over 30 minutes, with a tool pressure of 2000 mBar under vacuum. The temperature is held for an additional 30 minutes, and the sample is

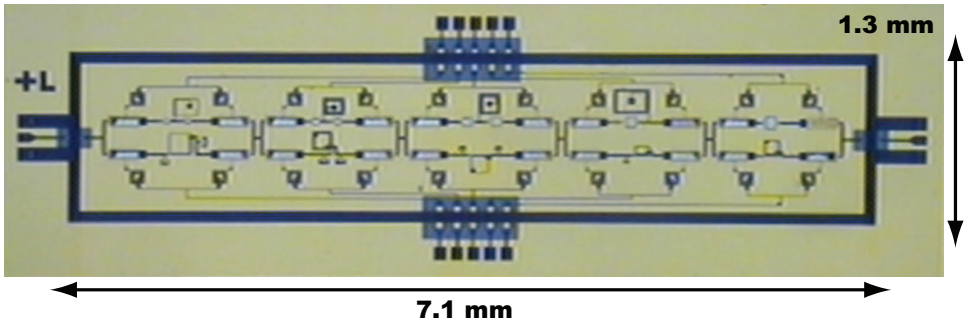

Figure 76: Microscope photograph of full five-bit phase shifter.

brought back to ambient temperature over 45 minutes.

Fig. 77 shows an SEM of a cavity on the cap with the 200 μm wide bond ring. This roughness visible on the cavity surface is a by-product of the etching process, but since it is 150 μm above the MEMS wafer it has no negative impact on performance.

Package quality was tested using the Military Standard 883G, Method 1014.12. This subjects the packaged device to 100% humidity at 100 °C for 10 hours, simulating approximately 10 years of lifetime in an accelerated environment [33, 41]. Working measurements after packaging confirm the MEMS devices have survived the bonding process and moisture testing.

Thermal compression bonding is a well understood packaging technology [25, 29, 30, 62, 69]. However, the advance of a micromachined base wafer and the interconnect method to achieve broad-band performance has allowed the mature thermal compression method to be adapted suitably to RF MEMS and RF MEMS circuit wafer-scale packaging.

7.9 Post-Packaging Measurements

Measured return loss and insertion loss for the packaged five-bit MEMS phase shifter can be seen in Figs. 78 and 79, respectively. The phase shifter maintains a return loss better than -10 dB for 8-12 GHz, with an average loss of 4.5 dB. The maximum loss is 8 dB at 8 GHz, with a loss variation of 2 dB across the phase states above 9.5 GHz. This variation in loss is again due to the higher amount of loss in the bits with larger inductors. The larger loss at lower frequencies is caused by the inductor performance in the high-pass filter section of the 11° bit. The smallest phase-shift bits are the most prone to fabrication tolerances [48],

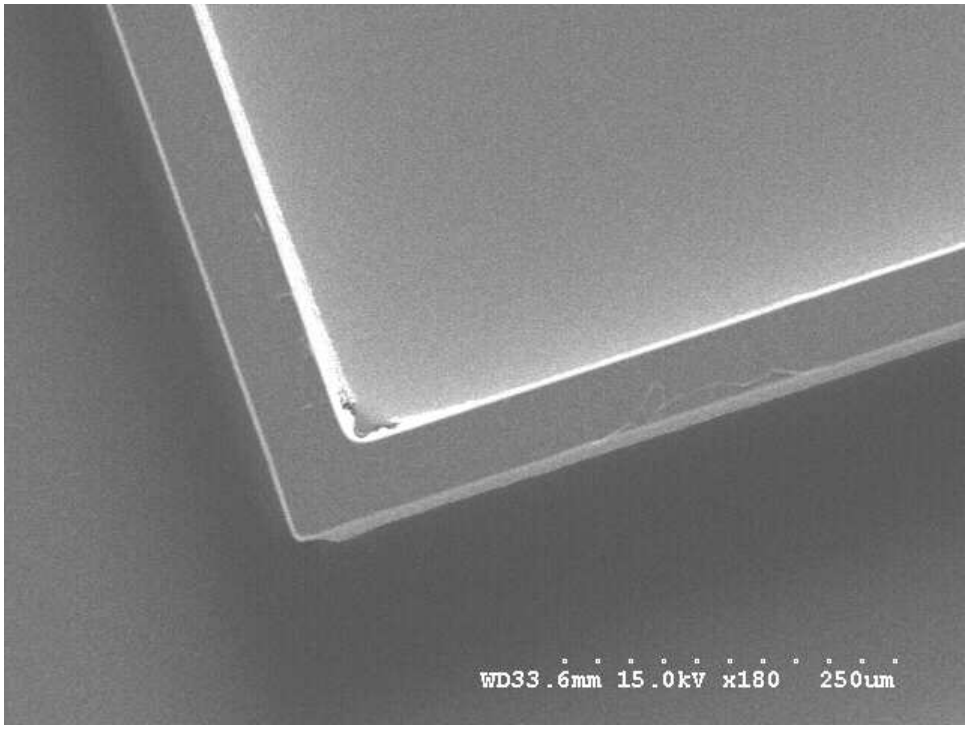

Figure 77: SEM of cap wafer showing 200 μm wide bond ring.

so this degradation in performance over the 4-bit phase shifter was expected.

Measured phase shift for all 32 states is seen in Fig. 80 with RMS phase error over frequency in Fig. 81. RMS phase error is similar (as 4 of the 5 bits are identical) yet slightly better than the 4-bit phase shifter, with 7° up to 11.3 GHz, and lower than 10° for all of X-band.

At 7.1 mm long and 1.3 mm wide measured at the bond ring, the full five-bit shifter has a die area of only 9.2 mm^2.

7.10 Summary

The first packaged MEMS-based High-pass/Low-pass phase shifter has been successfully demonstrated. The circuit can provide 360° of phase shift, with an RMS phase error less than ± 10° over the entire band of operation. The shifter achieves an average insertion loss of 4.5 dB, and maintains a return loss greater than 10 dB for all states over the band of operation. Total shifter die-area was 9.2 mm^2, slightly less than the 9.84 mm^2 un-packaged all-pi SiGe phase shifter presented earlier.

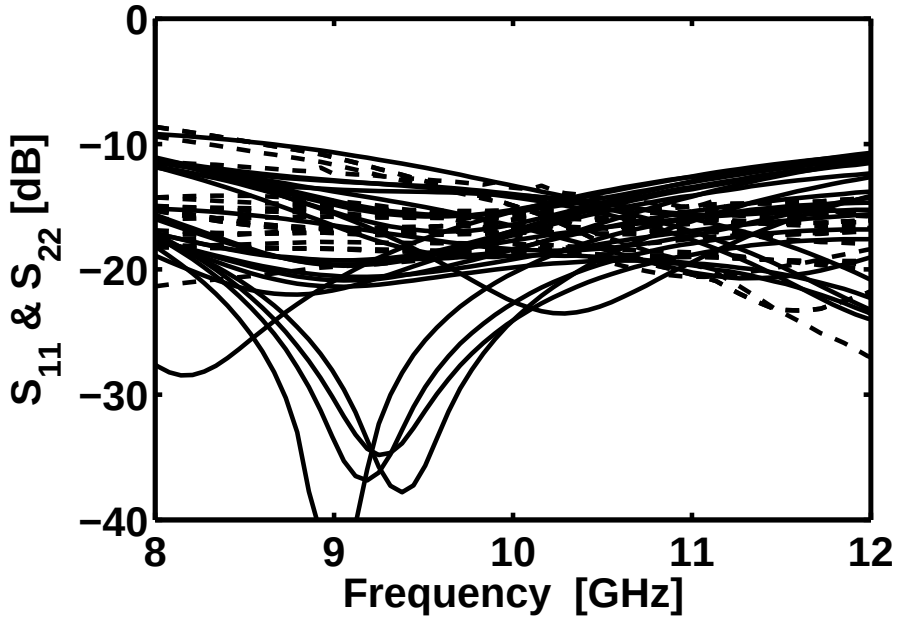

Figure 78: Input and output match for the packaged five-bit MEMS Phase Shifter.

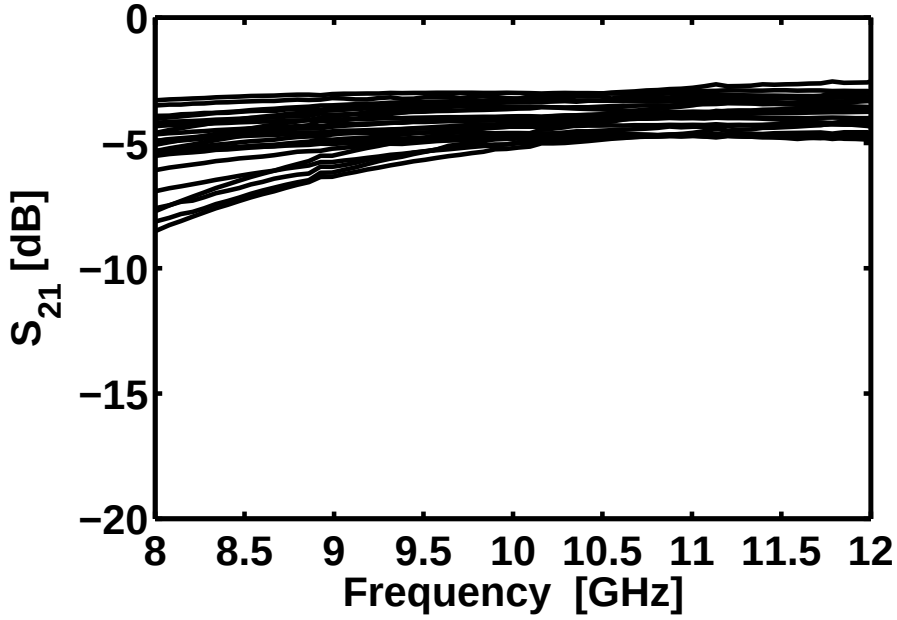

Figure 79: Insertion for the packaged five-bit MEMS Phase Shifter.

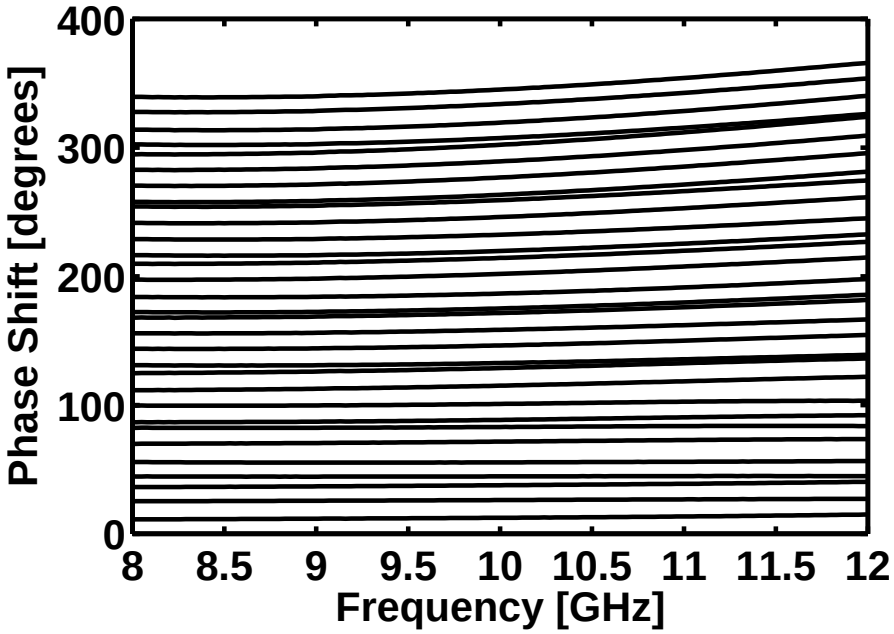

Figure 80: Phase Shifts for the packaged five-bit MEMS Phase Shifter.

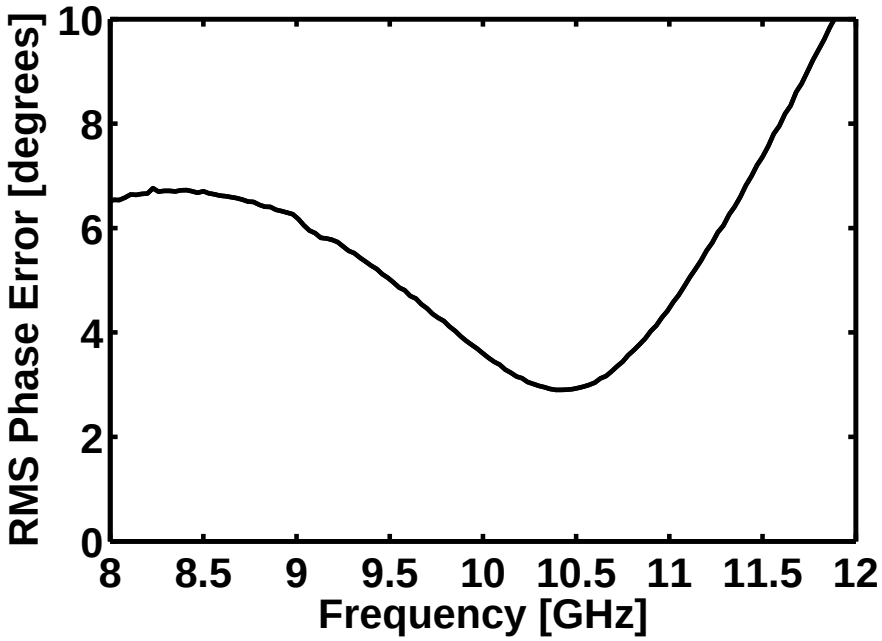

Figure 81: RMS Phase Error for the packaged five-bit MEMS Phase Shifter.

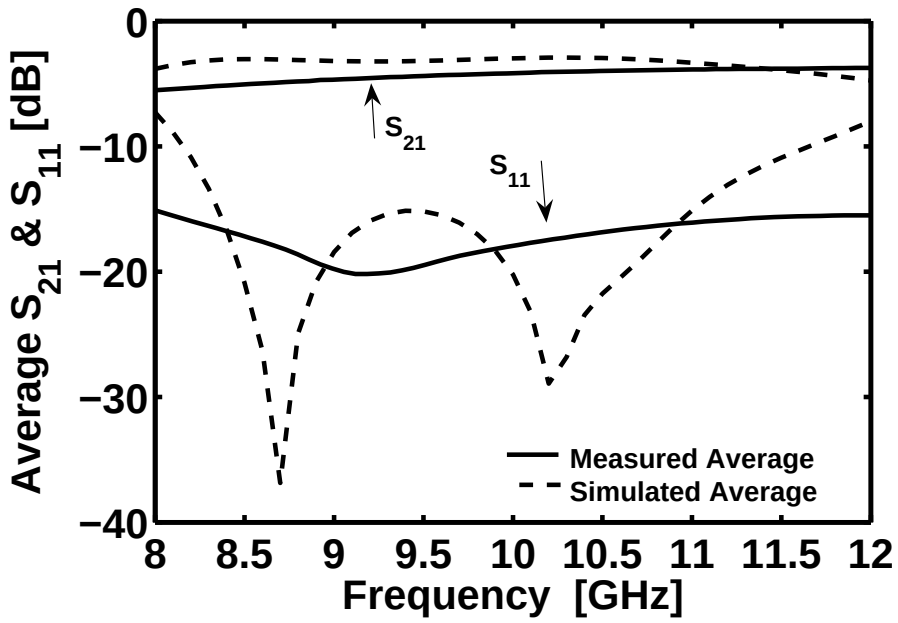

Figure 82: Measured and simulated average insertion and return loss for five-bit phase shifter.

This is a substantial improvement in the insertion loss over the transistor-based SiGe phase shifters, that averaged higher than 17 dB for the same five-bit topology. Further discussion on the advantages and disadvantages of MEMS and active SiGe will be discussed in the next chapter.

For a clean comparison between the measured a simulated performance, the average of the insertion and return loss across all states is shown in Fig. 82. Fabrication constraints required the metal layers in the inductors and capacitors to be thinner than expected during the simulation phase of the design. While the potentially higher loss was taken into account for phase error performance, the measured device showed slightly more loss and a less resonant return loss. However, given the complexity of full-wave simulation required and fabrication tolerances, the match between simulated and measured performance is excellent.

While the low insertion loss in both the four-bit and packaged five-bit phase shifter is a direct result of the RF MEMS switches, the highly competitive RMS phase error is perhaps a greater accomplishment. Simulated and measured RMS phase error for the five-bit phase

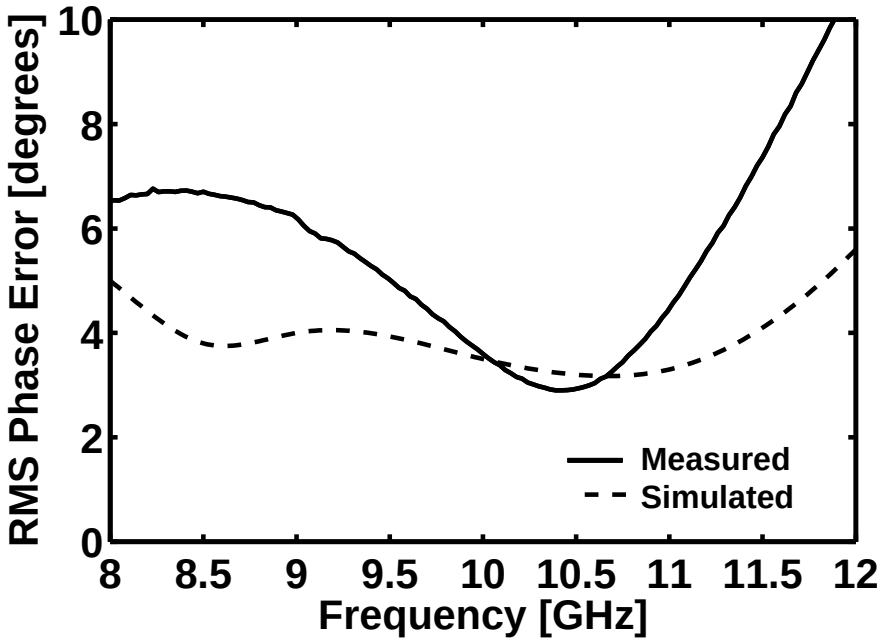

Figure 83: Measured and simulated RMS phase error for five-bit phase shifter.

shifter is compared in Fig. 83. The lack of any reliable models or toolkits for inductors, with the addition of a unpredictable non-commercial fabrication facility, generated a large amount of uncertainty in the phase behavior of the fabricated device. By understanding the impact of resistive losses, parasitic sources and fabrication shortcomings, these problems were overcome with careful modeling of the primary drivers of phase error and intelligent bit topology design and ordering.

A comparison of the main performance attributes of the MEMS-based phase shifters presented in this work to the current high-pass/low-pass state of the art is shown in Table 9. As with the SiGe transistor-based phase shifters, excellent phase error has been achieved, with superior loss and large signal performances. The comparison to the Raytheon and Hittite phase shifters is significant, as these were fabricated in a fully commercial (and hence, more predictable) facility.

Being the first MEMS-based phase shifter with the high-pass/low-pass topology, there are no competing MEMS-based designs for direct comparison. However, there are a variety of distributed time-delay phase shifters utilizing MEMS technology. A comparison of the

Table 9: Comparison of the MEMS-based phase shifters presented in this work to the state of the art using the high-pass/low-pass topology

	ϕ Error	Loss (dB)	Area (mm^2)	P_{1dB} (dBm)	IIP3 (dBm)	Note
Raytheon	25°	14	14	3	17	p-i-n
U. Michigan	20°	3.7**	1.1	-27.3	-17.3	Tunable
Hittite	10°	6.5	1.7	NR***	NR***	mHEMT
4-bit MEMS	10°	3	5.5	>30*	N/A	MEMS
5-bit MEMS	10°	4.5	9.2	>30*	N/A	MEMS

* determined by dielectric breakdown [6, 46, 73]. ** 3.7 gain, design incorporates LNA, *** NR: Not Reported. Sources: [10, 11, 24, 32, 66]

Table 10: Comparison of the MEMS-based phase shifters presented in this work to the state of the art using the high-pass/low-pass topology

	ϕ Error	Loss (dB)	Loss/bit (dB)	Area (mm^2)	Substrate	Topology
Raytheon	11°	2.2	0.55	82	Si	Reflect
U. Michigan	5°	1.2	0.6	18	Quartz	Loaded
GEDC	4°	0.96	0.24	67	LCP	Line
4-bit MEMS*	10°	3	0.75	5.5	Si	HPLP
5-bit MEMS*	10°	4.5	0.9	9.2	Si	HPLP

* average data over the entire 8-12 GHz band. Sources: [10, 11, 26, 35, 40]

main attributes of the state of the art in MEMS-based phase shifters of any topology is shown in Table 10.

This comparison is easily misleading, as the time delay types present phase error and loss for a set frequency only, while the phase error and loss of the high-pass/low-pass designs are given as the average for the entire 8-12 GHz band. The higher loss/bit of the high-pass/low-pass designs are a direct result of the very narrow transmission lines required by the 10 μm SiO_2 substrate. However, this apparent increase in loss is an acceptable tradeoff for the significant reduction in die-area required, critical for phased array systems utilizing many thousands of individual phase shifting circuits. The high-pass/low-pass topology, on average, is less than 10% of the size required by the state of the art in alternative topologies. This provides a large reduction in the overall cost and complexity of a phased array system.

CHAPTER VIII

ACTIVE SIGE AND MEMS PHASE SHIFTER COMPARISON

For an ideal comparison between the MOS- or HBT-based SiGe phase shifters and the MEMS-based design, the MEMS switches would be fabricated on the same SiGe sample either at the same time as the top metal layers or by post-processing. However, the cost and complexity of this given the available die space and limited supply made this impractical. By fabricating an in-house sample that accurately replicates the metal and dielectric layers used as the RF routing and passive layers, a fair comparison can be drawn between the active and MEMS approaches to the High-Pass/Low-Pass phase shifter. A comparison of the main attributes for the SiGe- and MEMS-based phase shifters is presented in Table 11.

Clearly, a significant decrease in insertion loss is achievable with MEMS technology. In addition, the lack of semiconductors overcomes the problems associated with linearity. While MEMS devices do not exhibit compression under high input power levels (as with the P_{1dB} in the MOS and HBT designs), they can suffer catastrophic damage at very high input power levels. This destruction is caused by the breakdown of the dielectric materials that compose the silicon nitride layer of the MEMS and of the capacitors. [73] However,

Table 11: Comparison of the SiGe and MEMS-based phase shifters presented in this work

	ϕ Error	Loss (dB)	Area (mm^2)	P_{1dB} (dB)	IIP3 (dB)	Note
4-bit MEMS	10°	3	5.5	>30*	N/A	MEMS
5-bit MEMS	10°	5	9.2	>30*	N/A	MEMS
4-bit SiGe	7°	12.3	9.6	5.7	20	HBT
4-bit SiGe	5°	17.2	8.1	8.6	21	MOS
5-bit SiGe	8°	18	9.9	4.4	18	HBT

* determined by dielectric breakdown [6, 46, 73].

this power level far surpasses that which the semiconductor based devices could survive.

While the MEMS-based phase shifter can easily be shown to be superior in many respects to transistor-based technologies, it is not without substantial drawbacks in a real world environment. Without proper packaging, the MEMS devices quickly degrade from moisture in the ambient environment. Packaging technologies exist that can alleviate this problem, but not without an increase in cost.

Dielectric charging remains a significant problem in the lifetime reliability of MEMS devices, causing them to permanently remain in the down state. While no commercially compatible solution to this problem has yet been found, new techniques to help develop a better understanding are being developed [77, 78]. Metal fatigue in the membrane can further limit the lifetime of MEMS devices. Current and future work in this area [15, 20, 73] will help remedy this problem with new materials and robust MEMS design.

Typical switch speeds for the popular MEMS topologies are on the order of 15 μs, 3-4 orders of magnitude slower than transistor based technology and possibly a great impediment to their use in radar applications. However, new technologies have made sub-microsecond speeds achievable [60].

Despite the many drawbacks, MEMS technology can currently provide the best loss and isolation performance. They may be found suitable for applications such as satellite-based radar, where power consumption and loss is a primary driver in system requirements. The benefits of low loss increase with higher frequency bands, as MEMS technology easily achieves less than 0.1 dB loss up to 110 GHz and beyond.

In time, the problems MEMS technology faces in a commercial environment may be largely overcome. However, at the present state of the art, the problems associated with reliability and switch speeds allow transistor-based High-Pass/Low-Pass phase shifters to remain the dominant architecture for phased array radar applications.

CHAPTER IX

CONCLUSION

The investigation of utilizing MEMS technology to design and fabricate the first MEMS-based High-pass/Low-pass phase shifter has been performed. Prior to this research, MEMS phase shifters had only been implemented in the limited-bandwidth transmission-line topologies. Prior High-pass/Low-pass phase shifters relied on lossy HBT, MOS and pin diode technologies. In this research, the niche of a low-loss, wide-bandwidth phase shifter has been populated.

A comprehensive study of the shortcomings associated the High-pass/Low-pass topology has been performed, increasing the understanding of error sources arising from bit layout issues and fabrication tolerances. This included a detailed analysis of error sources in monolithic microwave phase shifters due to device size limitations, inductor parasitics, loading effects, and non-ideal switches. Each component utilized in the implementation of a monolithic high-low pass phase shifter was analyzed, with its influence on phase behavior shown in detail. An emphasis was placed on the net impact on absolute phase variation, which is critical to the system performance of a phased array radar system. The design of the individual phase shifter filter sections, and the influence of bit ordering on overall performance was also addressed.

A variety of X-band four- and five-bit phase shifters were fabricated in a 200 GHz SiGe HBT BiCMOS technology platform, and further served to validate the analysis and design methodology. The SiGe phase shifter can be successfully incorporated into a single-chip T/R module forming a system-on-a-chip (SoC).

Reduction in the physical size of transmission lines was shown to be a possibility with spinel magnetic nanoparticle films. The signal transmission properties of phase lines treated with nanoparticle thin films were examined, showing the potential for significant size reduction in both delay line and High-pass/Low-pass phase topologies.

Wide-band, low-loss, and near-hermetic packaging techniques for RF MEMS devices were presented. A thermal compression bonding technique compatible with standard IC fabrication techniques was shown, that uses a low temperature thermal compression bonding method that avoids plastic deformations of the MEMS membrane. An alternative organic polymer based packaging solution was also addressed, the first localized-heating technique of its kind for LCP.

Ultimately, a system-on-a-package (SoP) approach was demonstrated that utilized packaged RF MEMS switches on high resistivity silicon to maintain the performance of the SiGe phase shifter with much lower loss. By increasing the depth of knowledge about the impact of resistive losses, parasitic sources and fabrication shortcomings, these problems were overcome with careful modeling of the primary drivers of phase error and intelligent bit topology design and ordering. The extremely competitive performance of the MEMS-based High-pass/Low-pass phase shifter, despite the lack of the extensive toolkits and commercial fabrication facilities employed with the active-based SiGe phase shifters, confirms both the effectiveness of the detailed phase error analysis presented in this work and the robust nature of the High-pass/Low-pass topology.

CHAPTER X

CONTRIBUTIONS

There have been many contributions to the academic and industry communities as a result of this work, both in advancing the state of the art and in increasing the understanding of the underlying mechanisms that continue to constitute speed-bumps on the road to progress. Perhaps the most substantial of these contributions are the following:

- The first MEMS-based High-Pass/Low-Pass phase shifter
- The first packaged MEMS-based High-Pass/Low-Pass phase shifter
- A comprehensive analysis of phase error sources for monolithic High-Pass/Low-Pass phase shifters
- A new hybrid topology providing lower loss and significantly less die area than previous work
- The first purely micromachined ultra-wide-band interconnect technology for RF MEMS eutectic bonding
- The first low-cost localized heating packaging technique for Liquid Crystal Polymer (LCP)

In addition, two testbeds have been designed and assembled, with fully automated test suites to provide a platform for further significant advancements in the future understanding of the following vital problems facing MEMS technology:

- Hot and cold lifetime reliability of RF MEMS switches
- Minimum actuation voltage and maximum switch speed behavioral tests over switch lifetime
- Dielectric charging and relaxation effects in RF MEMS switches

CHAPTER XI

PUBLICATIONS TO DATE

The following journal and conference papers have been accepted or are presently under review:

Journal Publications

- **Matthew Morton**, John Papapolymerou, "A MEMS-based 5-bit X-band Packaged High-Pass/Low-Pass Phase Shifter", Submitted to TMTT, April 2007.
- **Matthew Morton**, John Papapolymerou, "X-band 4-bit High-Pass/Low-Pass Phase Shifter with MEMS", Submitted to MWCL, April 2007.
- **Matthew Morton**, Jonathan Comeau, John Cressler, Mark Mitchell, John Papapolymerou, "A 5-bit, Silicon-based, X-band Phase Shifter Using a Hybrid pi/t High-pass/Low-pass Topology", Submitted to IEE Proceedings Microwaves, Antennas and Propagation, March 2007.
- **Matthew Morton**, Jonathan Comeau, John Cressler, Mark Mitchell, John Papapolymerou, "Sources of Phase Error and Design Considerations for the On-Chip High-Low Pass Phase Shifter", IEEE Transactions on Microwave Theory and Techniques, Vol 54, Issue 12, Part 1. Dec. 2006, pp 4032-4040.
- Jonathan Comeau, **Matthew Morton**, John Cressler, John Papapolymerou, Mark Mitchell, "A Comparative Study of SiGe HBT Versus CMOS Implementations of Fully-Integrated, High-pass/Low-pass, X-band Phase Shifters for Radar Applications" To be submitted to TMTT March 2006.
- Il Kwon Kim, Nickolas Kingsley, **Matt Morton**, Ramanan Bairavasubramanian, John Papapolymerou, Manos M. Tentzeris, and Jong-Gwan Yook, "Fractal Shaped Microstrip Coupled Line Bandpass Filters For Suppression Of 2nd Harmonic", IEEE

Transactions on Microwave Theory and Technique, Vol. 53, No. 9, pp. 2943-2948, Sept. 2005.

- **Matthew Morton** and John Papapolymerou, "Wide-band finite ground coplanar (FGC) interconnects for on-chip packaging of RF MEMS switches used in smart antennas and phased arrays", IEEE Antennas and Wireless Propagation Letters, Vol. 3, Issue 1, pp. 239=242, 2004.

- J. Andrews, **M. Morton**, Jongsoo Lee, J. Papapolymerou, J. D. Cressler, A.K. Sutton, B.M. Haugerud, P.W. Marshall, R.A. Reed, Daehyung Cho, "The effects of proton irradiation on the performance of mm-wave transmission lines implemented in SiGe technology", IEEE Transactions on Nuclear Science, Vol. 51, Issue 6, Part 2, pp. 3807-3810, Dec. 2004.

Conference Publications

- **M. Morton**, N. Kingsley, and J. Papapolymerou, "Low Cost Method for Localized Packaging of Temperature Sensitive Capacitive RF MEMS Switches in Liquid Crystal Polymer," to be presented at IMS 2007, June 2007.

- J. P. Comeau, **M. Morton**, J. D. Cressler, J. Papapolymerou, and M. Mitchell, "A highly-linear 5-bit, X-band SiGe HBT phase shifter," presented at IMS 2006, June 2006.

- **Matt Morton**, Guoan Wang, John Papapolymerou, "Wafer-scale packaging of RF MEMS for 50-90 GHz", Silicon Monolithic Integrated Circuits in RF Systems, 2006. Digest of Papers. 2006 Topical Meeting on 18-20 Jan., 2005 Page(s):32 - 34

- M. Morton, J. Andrews, J. Lee, J. Papapolymerou, J.D. Cressler, D. Cho, K. Hong, H. Shin, K. Park, S. Yi, "1n the design and implementation of transmission lines in commercial SiGe HBT BiCMOS processes", Silicon Monolithic Integrated Circuits in RF Systems, 2004. Digest of Papers. 2004 Topical Meeting on 8-10 Sept. 2004 Page(s):53 - 56

- Il Kwon Kim, Nickolas Kingsley, **Matt Morton**, John Papapolymerou, Manos M. Tentzeris, and Jong-Gwan Yook, "Fractal shape microstrip band pass filter on High Resistivity Silicon for Suppression 2nd Harmonics", Presented at the 35th European Microwave Conference in Paris, France, October 4-6, 2005.

- **Matt Morton**, C.R. Vestal, John Papapolymerou, Z.J. Zhang, "Fabrication and characterization of spinel magnetic nanoparticle thin film transmission lines", Microwave Conference, 2003. 33rd European Volume 3, 7-9 Oct. 2003 Page(s):1307 - 1309 Vol.3

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